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INTERNATIONAL EDITION
OCTOBER 16, 1986

EDN

Industrial Electronics Product Showcase

SCSI peripherals

Touchscreen displays

PC-based instruments

Synchronous V/F converters

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

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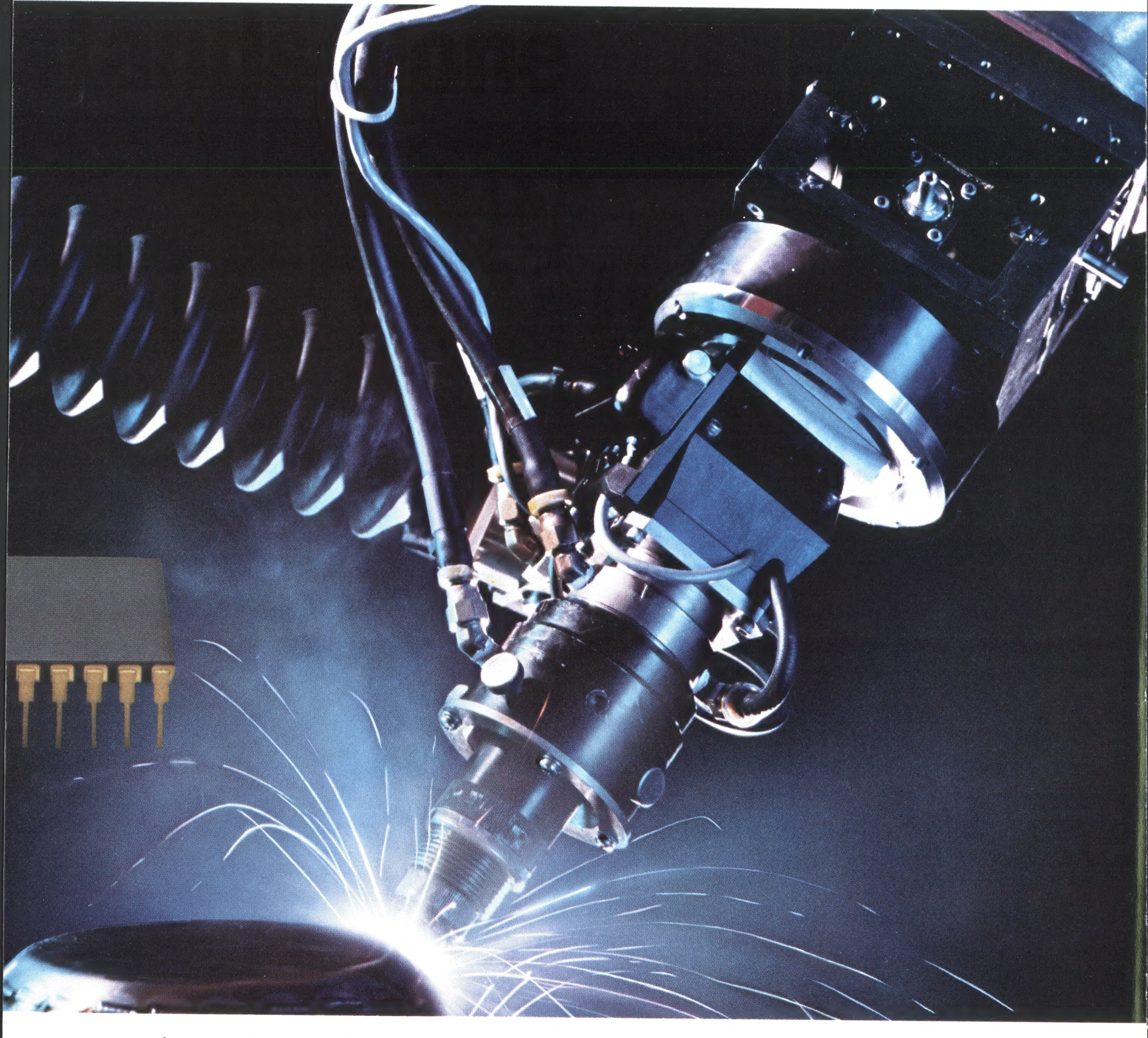
stands alone.



error correction technique, the ICL7134 provides up to 14 bits of accuracy and ultra-high stability over the entire operating temperature range. Plus the same cool low-power CMOS performance.

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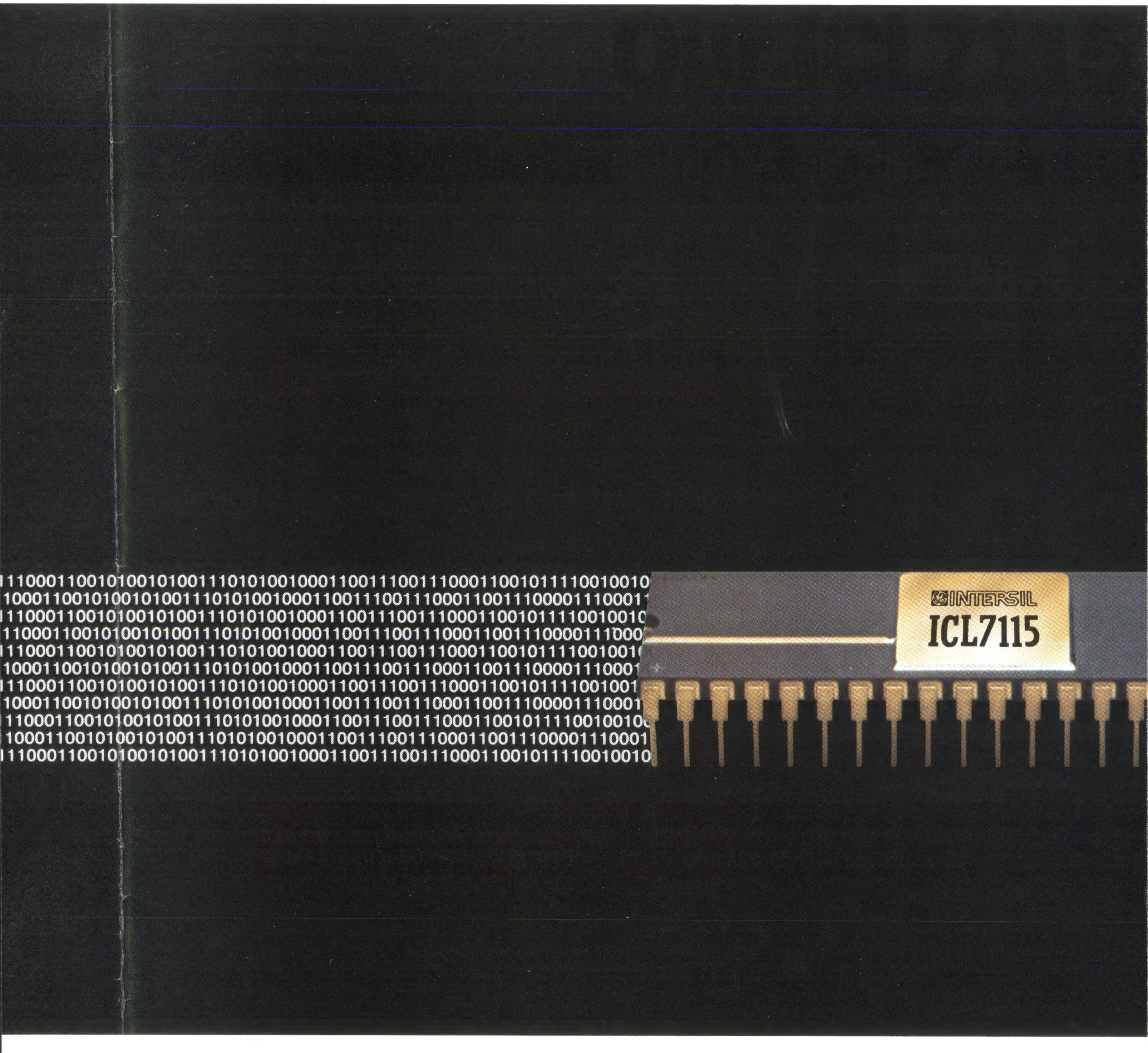

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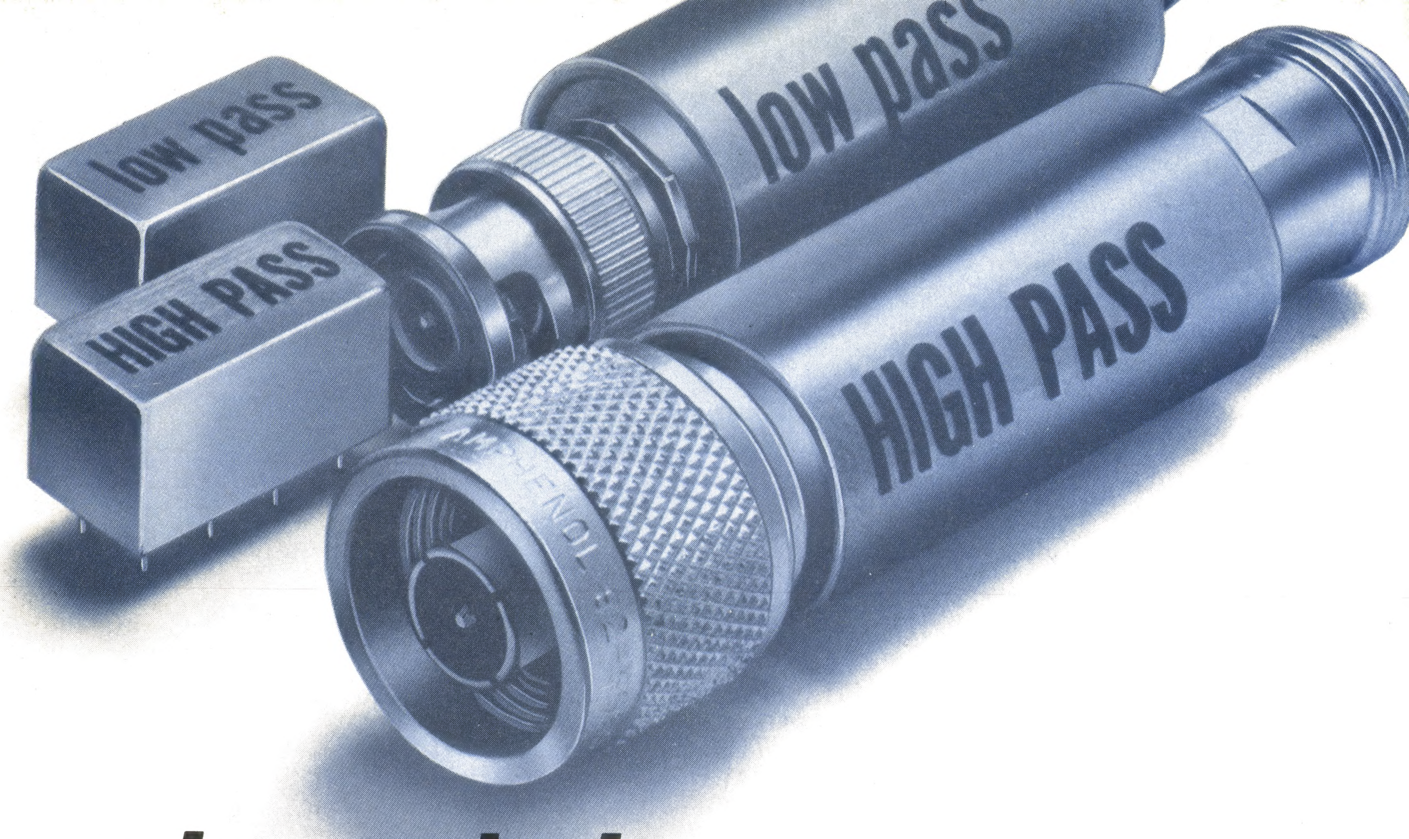

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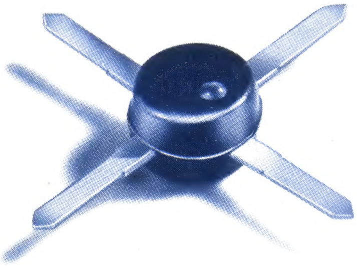

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CIRCLE NO 8

Volume 31, Number 21

EDN

October 16, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

***On the cover:** Manufacturers are unfolding new digital signal-processing chips that ease the implementation of complex algorithms. However, these chips also pose new design problems. See pg 162. (Photo courtesy Texas Instruments Inc; creative direction by Mary Ann Topezer; art direction by Kathryn L McElroy; photography by Kevin Hunter)*

DESIGN FEATURES

Special Report: DSP ICs 162

Choosing digital signal-processor chips isn't as difficult as it might seem. But beware: There are pitfalls along the way, from your first pencil sketch—where design subtleties await—to your implementation of an actual DSP task.—*Jon Titus, Senior Editor*

Designer's Guide to Synchronous V/F Converters—Part 1 183

By using a synchronous V/F converter (SVFC), you can design analog-input systems that have greater linearity than that attainable by using asynchronous V/F converters or A/D converters. In this article, first in a 2-part series, you'll become acquainted with V/F converters in general and the AD651 SVFC in particular.—*Larry Devito, Analog Devices Semiconductor*

Touchscreen displays suit multifarious applications 195

After 10 years of technical improvement and cost reduction, touch-sensitive screens have achieved price and performance levels that compare favorably with other computer-input devices. Given that, and the ultimate simplicity of the technology itself—the pointing of a finger—it's puzzling that more applications don't make use of it.—*John Javetski*

Designer's Guide to VME Bus Control—Part 2 211

By using fuse-programmable controllers (FPCs) and PLDs, you can implement VME Bus control in your computer system with a minimum of hardware. Part 1 (October 2, pg 187) of this 2-part series described the bus-arbitration process and control functions and showed how to implement the VME Bus protocol in an FPC. This final part describes the implementation of similar controllers for slave modules and interrupt handlers, and it provides tools for programming the FPC.—*Arthur Khu, Advanced Micro Devices*

Continued on page 7

EDN (ISSN 0012-7515) is published 45 times a year, biweekly with one additional issue in January, February, March, August, and December, two additional issues in April, June, July, September, and November, and three additional issues in May and October by Cahners Publishing, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158. William M Platt, President; Terrence M McDermott, Executive Vice President; Jerry D Neth, Vice President of Publishing Operations; J J Walsh, Financial Vice President/Magazine Division; Thomas J Dellamaria, Vice President Production & Manufacturing; Terrence McDermott, Group Vice President. Copyright 1986 by Reed Publishing USA, a division of Reed Holdings Inc; Saul Goldweitz, Chairman; Ronald G Segel, President and Chief Executive Officer. Circulation records maintained at Cahners Publishing Co, 270 St Paul St, Denver, CO 80206. Second class postage paid at Denver, CO 80202 and additional mailing offices. Postmaster: Send address changes to EDN, 270 St Paul St, Denver, CO 80206.

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EDN

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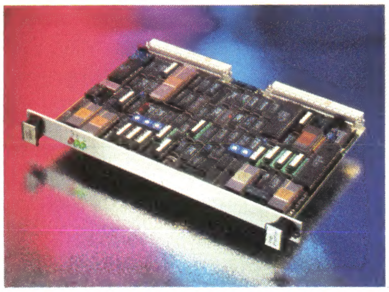
***PC-based modules and systems** bring the ease of front-panel instrument control to the task of programming instruments for benchtop testing or ATE applications (pg 61).*



***SCSI host adapters** suit a variety of VME Bus and Multibus system needs, but take care that the SCSI host adapter you choose is the best match for your application (pg 81).*

TECHNOLOGY UPDATE

High-level software simplifies use of PC-based instrument modules and systems 61

Manufacturers of personal-computer-based instruments recognize the value of shortened development times, and in their systems they have incorporated high-level software that lets you enter simple programming commands through "pseudo" front panels displayed on the personal computer's screen.—*Chris Everett, Regional Editor*

SCSI host-adapter boards meet the needs of Multibus and VME Bus computer systems 81

You buy, rather than design, boards to hurry a product to market, and now you can obtain Small Computer System Interface (SCSI) capabilities in board form for your system designs. SCSI host adapters suit a wide variety of VME and Multibus I systems needs, and they'll soon serve Mutibus II needs as well.—*Maury Wright, Regional Editor*

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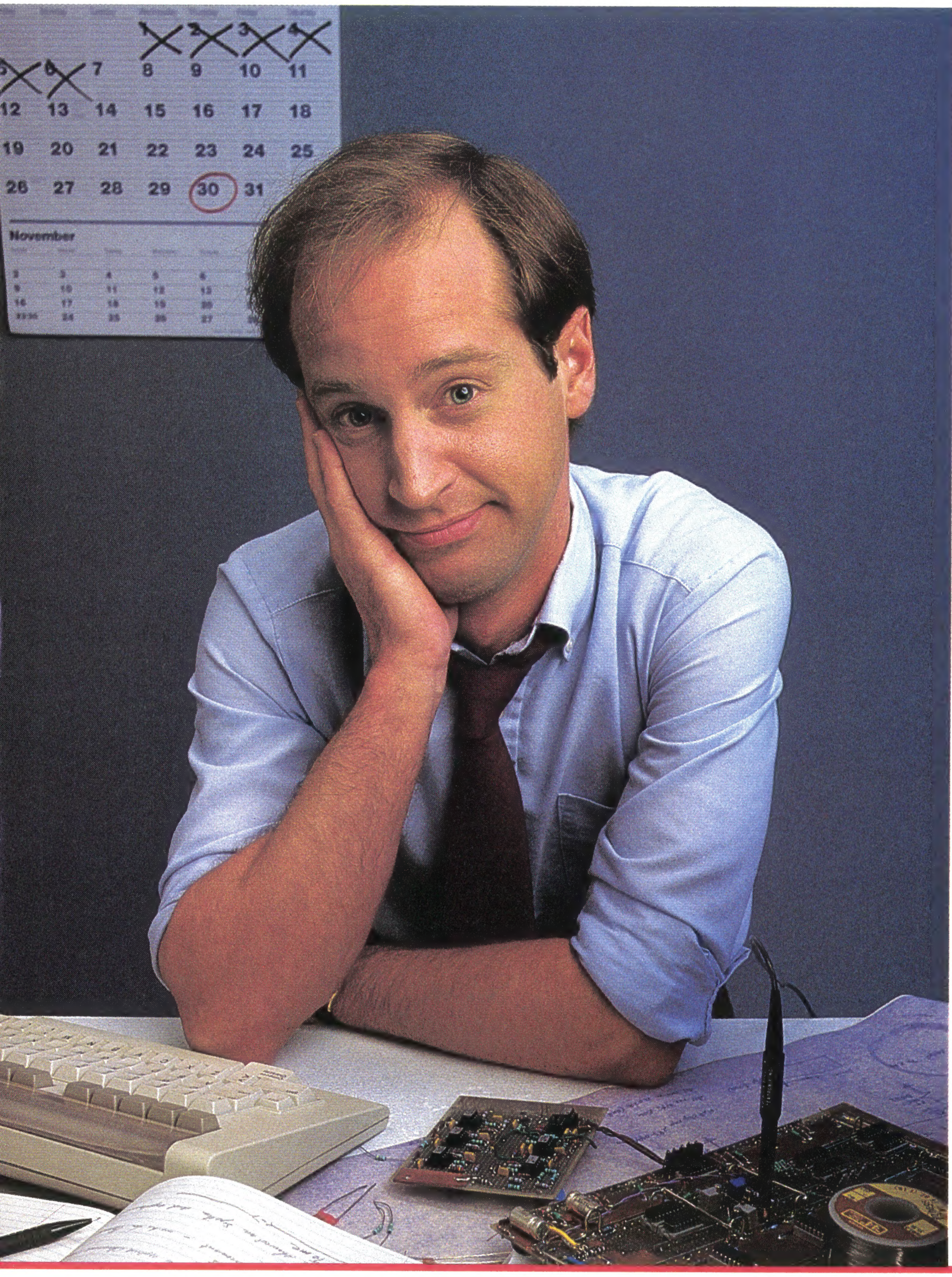

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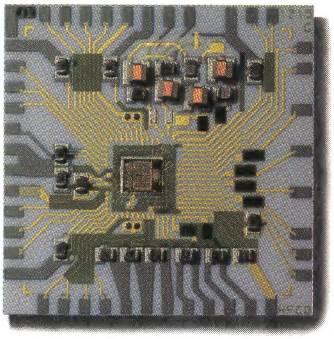

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October 16, 1986

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A computer should serve to amplify the skills that you and your colleagues possess, but make sure you can determine the point at which it becomes nothing more than a crutch.

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Support organizations for inventors takes the loneliness out of creating.—*Deborah Asbrand, Staff Editor*

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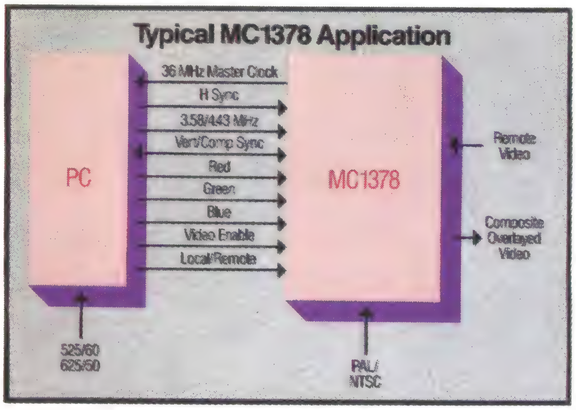

Display two composite color video signals together in overlay format.

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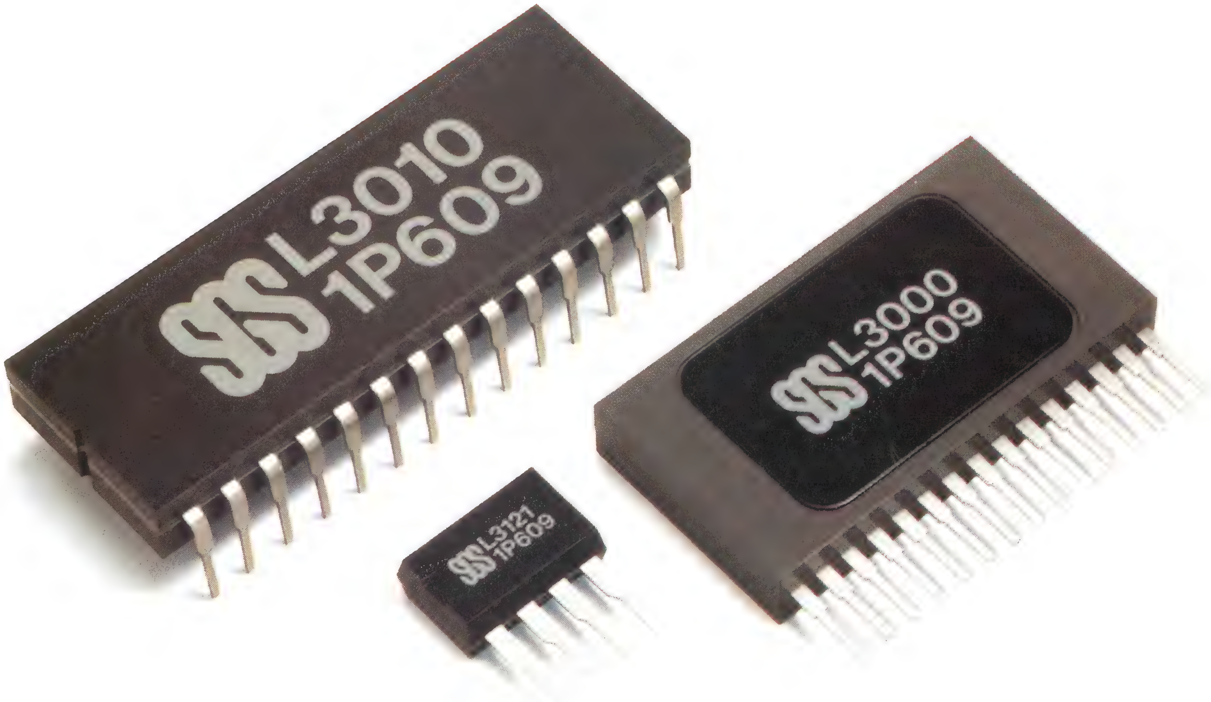

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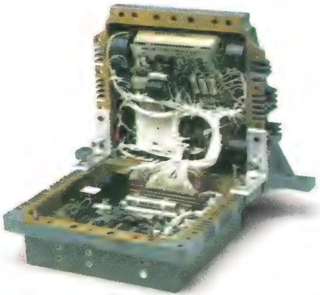

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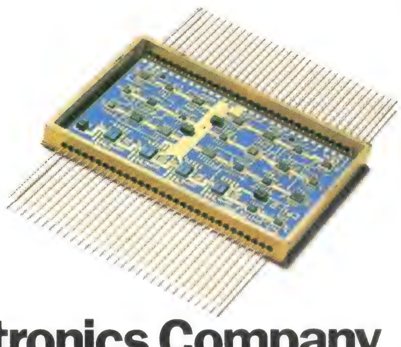

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STOP WISHING FOR THE IMPOSSIBLE IN DIGITAL ANALYSIS!

1
Complex, state-driven triggering at 200 MHz.

2
Symbolic, real-time software debugging.

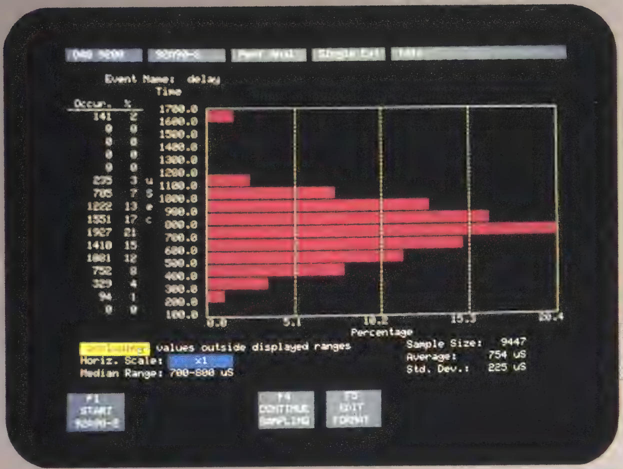
3
Simultaneous integration of multiple microprocessors.

4
100 + channels of acquisition at 2 GHz.

5
Easy ASIC device verification at up to 50 MHz.

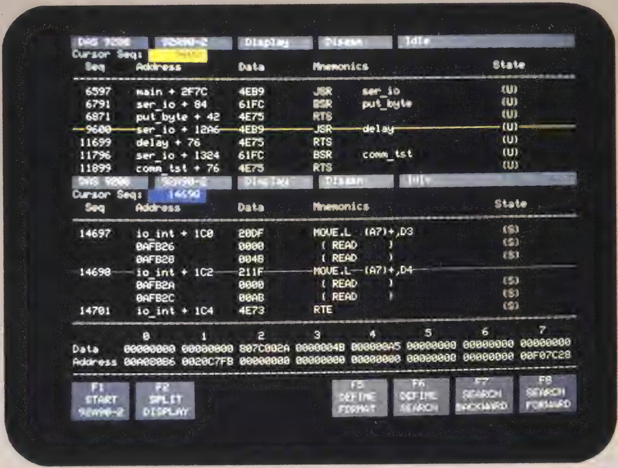
6
Functional board testing at an affordable price

INTRODUCING THE DAS9200: NOW TEK MAKES THE IMPOSSIBLE LOOK EASY.



```
        Event Name:  delay
                     Time
Occur.   %
  141    2        1700.0
    0    0        1600.0
    0    0        1500.0
    0    0        1400.0
    0    0        1300.0
    0    0        1200.0
  235    3  u     1100.0
  705    7  s     1000.0
 1222   13  e      900.0
 1551   17  c      800.0
 1927   21         700.0
 1410   15         600.0
 1081   12         500.0
  752    8         400.0
  329    4         300.0
   94    1         200.0
    0    0         100.0
                      0.0      5.1      10.2      15.3      20.4
                                   Percentage
           values outside displayed ranges        Sample Size:    9447
Horiz. Scale:    x1                               Average:       754 uS
Median Range: 700-800 uS                          Std. Dev.:     225 uS
```

Software Performance Analysis, like this distribution of a subroutine's execution times, helps you easily understand the activity of your code.



```
Cursor Seq:
 Seq     Address          Data       Mnemonics                    State
-----------------------------------------------------------------------
 6597    main + 2F7C      4EB9       JSR       ser_io             (U)
 6791    ser_io + 84      61FC       BSR       put_byte           (U)
 6871    put_byte + 42    4E75       RTS                          (U)
 9600    ser_io + 12A6    4EB9       JSR       delay              (U)
11699    delay + 76       4E75       RTS                          (U)
11796    ser_io + 1324    61FC       BSR       comm_tst           (U)
11899    comm_tst + 76    4E75       RTS                          (U)
Cursor Seq:    14698
 Seq     Address          Data       Mnemonics                    State
-----------------------------------------------------------------------
14697    io_int + 1C0     20DF       MOVE.L  (A7)+,D3             (S)
         0AFB26           0000        ( READ     )                (S)
         0AFB28           0048        ( READ     )                (S)
14698    io_int + 1C2     211F       MOVE.L  (A7)+,D4
         0AFB2A           0000        ( READ     )                (S)
         0AFB2C           00AB        ( READ     )                (S)
14701    io_int + 1C4     4E73       RTE                          (S)
-----------------------------------------------------------------------
             0        1        2        3        4        5        6        7
Data     00000000 00000000 807C002A 0000004B 000000A5 00000000 00000000 00000000
Address  00A000B6 0020C7FB 00000000 00000000 00000000 00000000 00000000 00F07C28
```

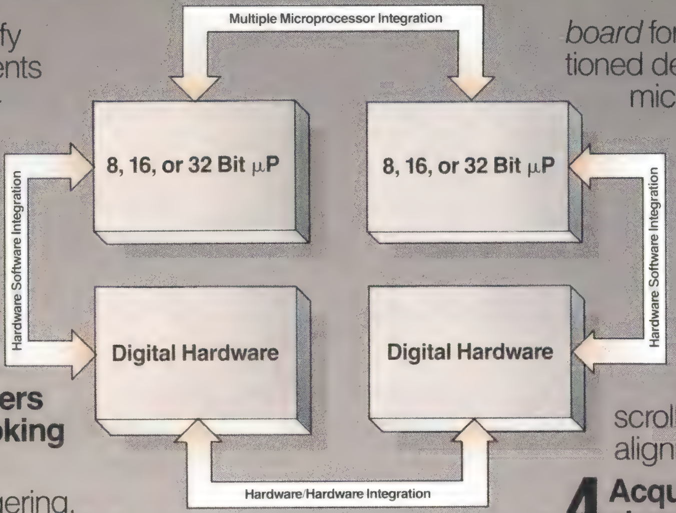
Step backwards through acquired data, including subroutines, stack and register models, using time-correlated split-screen displays to pinpoint problems.

In every dimension—speed, channel width, memory depth, trigger capability, modularity and ease of use—the DAS9200 dwarfs what's been possible before.

The DAS9200 features a tightly coupled, high-speed architecture in which multiple card modules can act as a single unit. Large color-coded displays, pop-up menus, performance analysis graphs, multi-tasking and more combine to uncomplicate logic analysis.

1 Apply state-driven triggering at 200 MHz with up to 384 channels of sync and async data acquisition.

You can assurance-test high-speed logic at full speed, using 4-level state tracking and high speed counter/timers integrated into the 92A16 timing board.


Multiple Microprocessor Integration
8, 16, or 32 Bit μP
8, 16, or 32 Bit μP
Hardware Software Integration
Hardware Software Integration
Digital Hardware
Digital Hardware
Hardware/Hardware Integration

You can monitor and verify all the timing measurements in a circuit, including setup and hold time, minimum pulse width, and precharge time, and quickly select commontest routines from the Trigger Library.

2 Register deduction and stack simulation let developers debug software by looking backwards in time.

Use the complex triggering, data qualification and 32K per channel memory of the 92A60/92A90 acquisition modules to monitor software activity in real time.

Continually updated register and stack displays let you quickly identify problems like stack overflow or incorrectly restored pointers—without breakpoints and manual notation.

3 Split-screen time-correlated displays help you monitor and correlate up to six microprocessors at once.

Take the same system modules used in debugging the hardware and software and reconfigure them *from the keyboard* for integrating partitioned designs or multiple microprocessors.

Use the dual timebases and real-time handshaking between modules to set up split-screen displays of disassembly with timing or state table data. Lock the two cursors so that both screens scroll in precise time alignment.

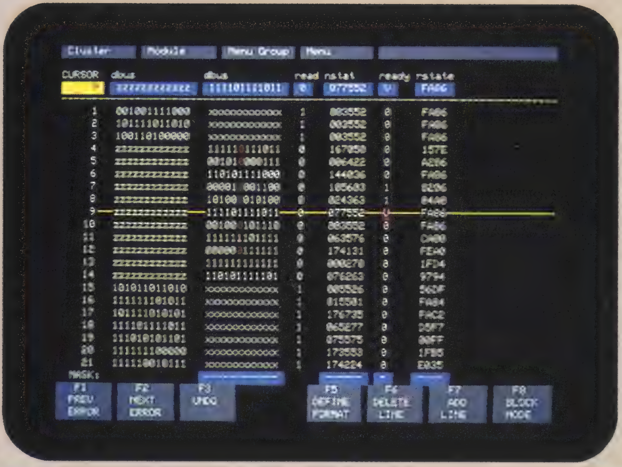
4 Acquire up to 160 channels at a full 2 GHz for unprecedented 500 ps sampling.

The 9200 offers the first acquisition unit to split the nanosecond: the 92HS8. With its 500 ps sample interval and 1.5 ns glitch detection, you can identify previously undetectable race conditions, spurious clocks and setup/hold violations in any logic family.

The 92HS8 is complemented by the world's most advanced probing system, featuring an input capacitance of less than 1 pf.

Available in desktop and rackmount versions, the DAS9200 mainframe can be augmented with up to three expansion mainframes for a total of 28 card slots.

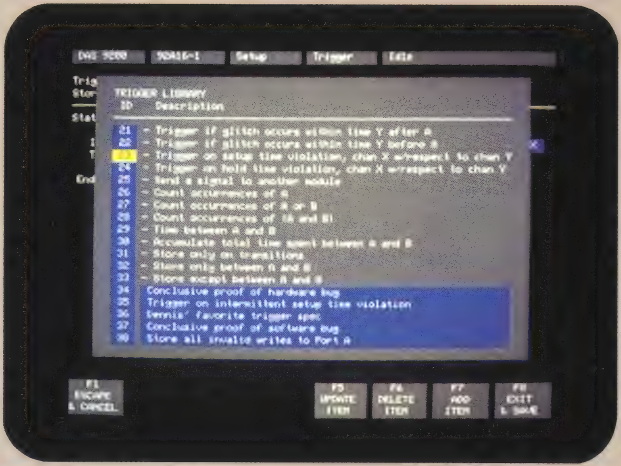
BENCHTOP ASIC OR PCB TESTS? YOUR WISH IS OUR COMMAND!



```
CURSOR  dbus           dbus          read  nstat   ready  rstate
   9    zzzzzzzzzzzzz  111101111011   0    077552    V     FA86

    1   001001111000   xxxxxxxxxxxx   1    003552    0     FA86
    2   101111011010   xxxxxxxxxxxx   1    003552    0     FA86
    3   100110100000   xxxxxxxxxxxx   1    003552    0     FA86
    4   zzzzzzzzzzzzz  111110111011   0    167050    0     157E
    5   zzzzzzzzzzzzz  001010000111   0    006422    0     A286
    6   zzzzzzzzzzzzz  110101111000   0    144036    0     FA86
    7   zzzzzzzzzzzzz  00001 001100   0    105603    1     8206
    8   zzzzzzzzzzzzz  10100 010100   0    024363    1     8408
    9   zzzzzzzzzzzzz  111101111011   0    077552    V     FA86
   10   zzzzzzzzzzzzz  00100 101110   0    003552    0     FA86
   11   zzzzzzzzzzzzz  111111101111   0    063576    0     CA00
   12   zzzzzzzzzzzzz  00000 111111   0    174131    0     FEA0
   13   zzzzzzzzzzzzz  111111111111   0    000270    0     1FD4
   14   zzzzzzzzzzzzz  110101111101   0    076263    0     9794
   15   101011011010   xxxxxxxxxxxx   1    005526    0     562F
   16   111111101011   xxxxxxxxxxxx   1    015501    0     FA84
   17   101111010101   xxxxxxxxxxxx   1    176735    0     FAC2
   18   111101111011   xxxxxxxxxxxx   1    065277    0     D5F7
   19   111010101101   xxxxxxxxxxxx   1    075575    0     00FF
   20   111111000000   xxxxxxxxxxxx   1    173553    0     1F85
   21   111110010111   xxxxxxxxxxxx   1    174224    0     E035
MASK:
```

Results of the ASIC prototyping system can be displayed in timing or state format, with differences from expected results clearly highlighted.



```
TRIGGER LIBRARY
 ID   Description
 21 - Trigger if glitch occurs within time Y after A
 22 - Trigger if glitch occurs within time Y before A
 23 - Trigger on setup time violation, chan X w/respect to chan Y
 24 - Trigger on hold time violation, chan X w/respect to chan Y
 25 - Send a signal to another module
 26 - Count occurrences of A
 27 - Count occurrences of A or B
 28 - Count occurrences of (A and B)
 29 - Time between A and B
 30 - Accumulate total time spent between A and B
 31 - Store only on transitions
 32 - Store only between A and B
 33 - Store except between A and B
 34   Conclusive proof of hardware bug
 35   Trigger on intermittent setup time violation
 36   Dennis' favorite trigger spec
 37   Conclusive proof of software bug
 38   Store all invalid writes to Port A
```

With the Trigger Library, you don't need to know the microprocessor microcode or the bits and bytes of trigger setup to tackle once-difficult problems.

5 The DAS9200 is available as a low-cost turnkey ASIC device verification system.

Featuring 50 MHz pattern generation, 8K bit vector depth, 1 ns edge placement and 0.5 V/ns slew rates, it is an accessible, easy-to-use alternative to centralized systems.

You can link to popular logic simulators, download test vectors, call up split-screen displays and analysis graphs, utilize multiple sets of patterns and parameter sweeps, and display results in timing or state format, with anomalies clearly highlighted.

6 The DAS9200 frees circuit board functional testing from costly and complicated central test systems.

Configure up to 1008 channels of stimulus at 50 MHz with 8K bits/channel of pattern memory. Up to 540 channels of acquisition at 20 MHz with 32K bits/channel memory. Or many other combinations.

Time-correlated module interactions let you use data acquired by one acquisition or stimulus module to change the activity of another for more realistic conditional testing... all for under $700 per I/O pin!

Compare your wish list against the complete list of DAS9200 capabilities. Contact your Tek sales engineer for the full story and the hands-on proof. Or call toll-free for more information.

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NEWS BREAKS

EDITED BY JOAN MORROW

JITTER ATTENUATOR IC INCREASES CAPACITY OF TOKEN-RING LAN

By removing as many as three unit intervals of the jitter that accumulates in 4-MHz IEEE-802.5 token-ring networks as data passes around the ring, the CSC80600 from Crystal Semiconductor (Austin, TX, (512) 445-7222) can almost double the LAN's current capacity. The 80600 is a physical-layer solution that uses an internal phase-lock loop and an 8-symbol FIFO elastic store. When used in station adapter cards, active wiring concentrators, or repeater devices, the 80600 accepts 8-MHz clock and Manchester data inputs, removes as many as 1.5 data bits of jitter, then furnishes the data and clock signals. Available in a 14-pin DIP, the 80600 costs $8 (1000).—J D Mosley

CMOS ARRAYS EXCEED 9000 GATES AND FEATURE DESIGN MANUALS

AMCC (San Diego, CA, (619) 450-9333) has added a 1.5-μm CMOS gate-array family to its product offerings. The Q9000 Series includes arrays with 2200 to 9300 gates, and all family members have intrinsic gate delays of less than 0.5 nsec. The arrays feature 90-MHz toggle frequencies and dissipate less than 18 pW per gate per MHz. Input/output pair delay is 4 nsec for TTL interfaces and 3.2 nsec for CMOS interfaces. Expect eight- to 10-week cycle times from completion of logic simulation to delivery of prototypes. The arrays range in price from $15 to $95 (10,000).

AMCC also offers the Micromatrix Design Manuals for engineers designing with its bipolar or CMOS arrays. The manuals feature an array-specific section with information such as design methodology, timing analysis, and power and packaging data. Another section covers workstation-specific topics.—Maury Wright

SINGLE-CHIP 212A MODEM INCLUDES UART AND LINE HYBRID

Supporting both 300- and 1200-bps, full-duplex operation, the Am79C12 single-chip modem from AMD (Sunnyvale, CA, (408) 732-2400) incorporates a UART and a 4-to-2 wire hybrid. These devices allow the modem to couple directly to a μP bus and, through a protective line interface, to the telephone line. The modem provides an interrupt input, which you can connect to its ring indicator output to support autoanswer operation; the modem also aids call-progress-tone detection by presenting received tone cadences on both a carrier-detect output pin and an internal status bit. The device directly supports DTMF tone dialing and allows pulse dialing through an output pin that you connect to the on/off hook lead of the protective line interface. Currently available in a 40-pin DIP, the Am79C12 costs $48 (100).—Steven H Leibson

5¼-IN. TAPE DRIVE STORES 2G BYTES ON 8-mm CARTRIDGE

The EXB-8200 tape subsystem from Exabyte Corp (Boulder, CO, (303) 442-4333) stores 2.152G bytes of information on a standard 120-min, 8-mm video tape cartridge with an error rate of one in 10^{12} bits. Both the tape drive and controller are packaged in a standard, full-height, 5¼-in. floppy-disk-drive format. The integral controller's SCSI interface transfers data at a 1.5M-byte/sec burst rate from its onboard 512k-byte buffer and sustains a transfer rate of 246k bytes/sec. You'll be able to obtain evaluation units by January, but you can preview the device at Exabyte's Comdex booth next month. The EXB-8200 will cost less than $1500 (10,000).—Steven H Leibson

CHIP MONITORS μP FUNCTIONS TO ENSURE CORRECT SOFTWARE EXECUTION

Acting as a watchdog for system malfunctions, the DS1232 from Dallas Semiconductor (Dallas, TX, (214) 450-0400) is an IC that monitors a microprocessor's power supply, its software execution, and external reset signals. It assumes that an out-of-

◄ For More Information on
Tektronix, Circle No. 1

tolerance condition indicates the existence of a system malfunction, then halts and restarts the μP after 250 msec to ensure a stabilized reset. To check for an adequate power supply, the DS1232 tests for input voltages below a programmable −5 or −10% of an on-chip reference voltage. The chip uses a software checkpoint to monitor routine software execution. Reset signals that are external to the μP go through the DS1232, which debounces the signal and enforces a 250-msec delay before restarting the μP. Available in an 8-pin DIP package, the DS1232 costs $3.60 (100).—J D Mosley

CMOS TIMERS RUN ON 1V, ARE PIN COMPATIBLE WITH 555, 556

The TLC551 and TLC552 CMOS timer pair from Texas Instruments (Dallas, TX, (800) 232-3200) are pin compatible with the widely used NE555 single and NE556 dual timer ICs but operate from power supplies from 1 to 18V. Both devices offer outputs that swing rail to rail, sink 100 mA, and source 10 mA. The TLC551 and TLC552 operate at frequencies to 1.8 MHz, are available in DIP and small-outline IC packages, and cost $0.90 and $1.70 (100), respectively.—Steven H Leibson

BULLETIN-BOARD SYSTEM OFFERS ASSEMBLERS AND ASSISTANCE

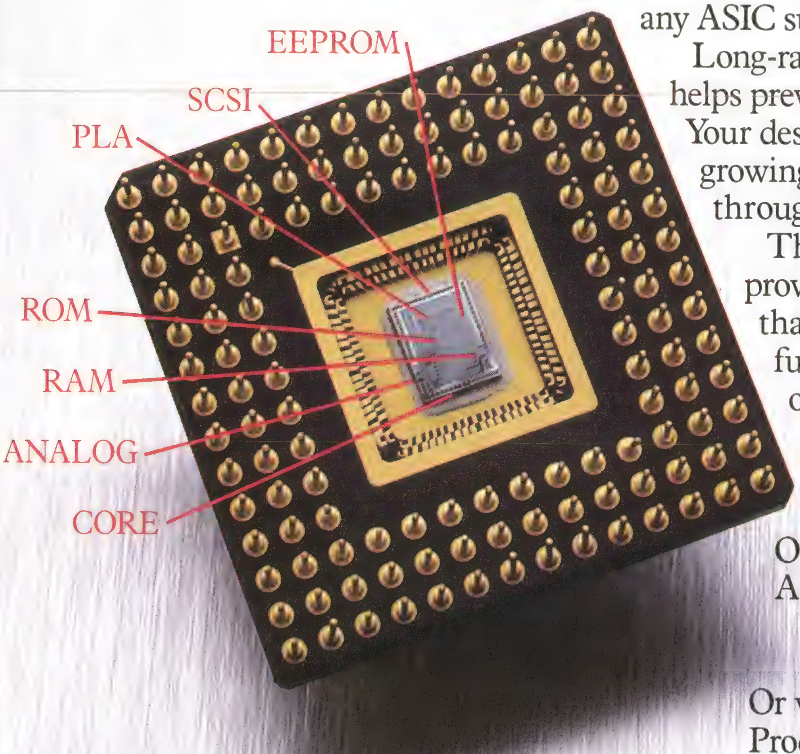
Dial-A-Helper, a free bulletin-board system run by National Semiconductor, provides tools and assistance for product developers using the company's μP and microcontroller products. The bulletin-board system contains assemblers for the NS455 family of terminal-management processors, the 16-bit NS16040 high-performance controller, and the COPS series of 4-bit microcontrollers. You can download assemblers for these products from the bulletin-board system for CP/M or MS-DOS operating systems as well as sample programs illustrating the assemblers' syntax. Your computer can telephone Dial-A-Helper at (408) 739-1162.—Steven H Leibson

CMOS IC DRIVES 33 LCD SEGMENTS WITHOUT MULTIPLEXING

The MC145453 LCD driver IC from Motorola (Austin, TX, (512) 928-6880) lets you directly drive as many as 33 LCD segments, thus providing a wider viewing angle and improved contrast compared with multiplexed displays. This CMOS IC has a 36-stage shift register and uses a serial binary input format. Specified over −40 to +85°C, the MC145453 has a segment drive current of 20 μA and a 3 to 10V operating voltage range. A 40-lead plastic DIP version costs $3.57, and a 44-lead, plastic leaded chip carrier model is $4.64 (500).—J D Mosley

THICK-FILM LINEAR POTENTIOMETER SENSES POSITION AND FORCE

Based on proprietary force-sensing-resistor (FSR) technology, a low-profile (0.015-in.) potentiometer developed by Interlink Electronics (Santa Barbara, CA, (805) 965-5155) senses both position and force. The device consists of a thick film of polymer with conductive fingers at each end screened onto a Mylar backing; the polymer's resistance will change linearly with pressure. A matching film of polymer with one conductive finger (which acts as the potentiometer's wiper) is laid face down over the first. Any pressure on the sandwich decreases the device's total resistance between the two conductive fingers at either end; the drop in resistance indicates the pressure. Pressure on the sandwich also decreases the resistance from the wiper finger to the finger at either side, indicating position. Resistance ranges from 10 MΩ down to 1 kΩ typ; the force range is from 20 gm/cm^2 typ. An evaluation kit costs $30.—Margery S Conner



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CIRCLE NO 17

16k-BIT ECL RAMs HAVE 10-nSEC MAX ACCESS TIME

Two types of 16k-bit ECL RAMs from Fujitsu feature maximum address access of 10 nsec and maximum chip-select access time of 5 nsec. One device works from −5.2V and the other works from −4.5V. Fujitsu fabricated the 4096-word×4-bit memories using 1.0-μm design rules and its U-shaped isolation method called the IOP-II. The 5.5×3.8-mm chips accommodate approximately 70,000 elements. Samples are available for ¥13,000 ($84) each.

1-CHIP 8-BIT μC HAS BUILT-IN EEPROM

Designed specifically for use in IC cards, the MSM61580 single-chip microcomputer from Oki Electric Industry Co incorporates a 16k-bit EEPROM. The 5.0×4.5-mm device, which was jointly developed with US manufacturer Catalyst Semiconductor, also furnishes 3k bytes of programmable ROM, 512 bytes of ROM, a 4.9-MHz clock frequency, and a 813.8-nsec execution time. The device can accommodate as many as 95 instructions. It sells for approximately ¥1200 ($7.74) (100,000).

20-km OF REPEATERLESS TRANSMISSION ACHIEVED WITH LED

By using a single-mode optical fiber and an LED that generates light from its surface edge, Fujitsu Ltd has succeeded in transmitting data at 600M bps for a distance of 20 km without a repeater device. Because the cost of the LED light source is about a tenth of that of a laser, the new prototype could become an economical communication system for high-speed local-area networks as well as public networks.

A problem with using LEDs for optical communication is linking the light generated from the LED's surface area to the ultrathin single-mode fiber whose cross-section diameter measures less than 10 μm. Fujitsu developed an LED that emits a 1.3-μm-wavelength light from the edge of the surface, allowing the light to focus into the fiber. The company also combined a gallium arsenide FET drive circuit and a compensation circuit to develop its prototype system.

1986 DEMAND FOR CVD, EPITAXIAL SYSTEM TO DECLINE 40%

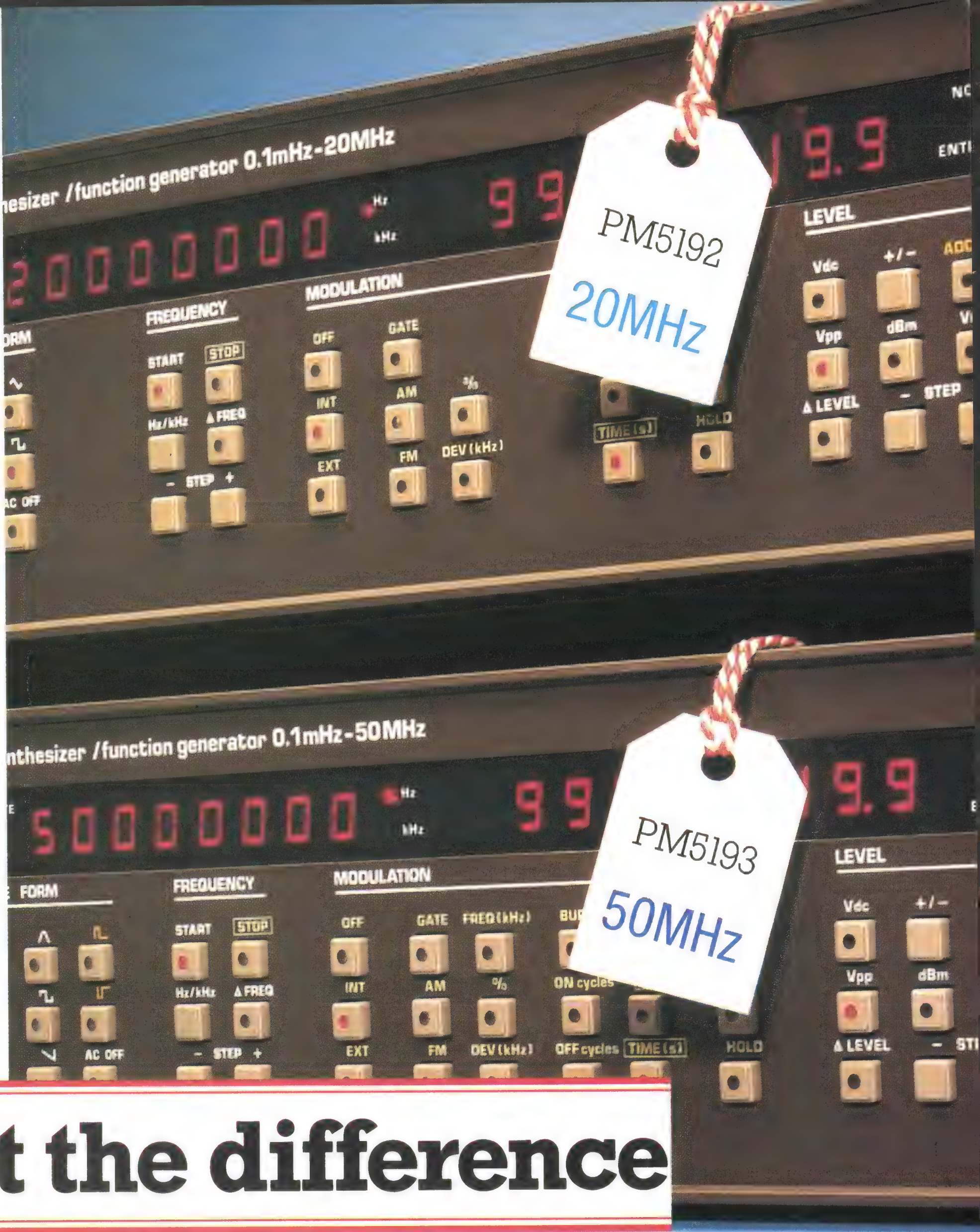
According to a report by Japan's semiconductor production equipment manufacturing industry, the 1986 demand for chemical-vapor-deposition (CVD) systems and epitaxial systems could drop drastically because of a decline in capital investments. The decline is due to a combination of several factors: the rise in value of the yen, trade frictions, and general economic conditions.

The size of the market for CVD systems could shrink 39% from last year to $104 million; the demand for epitaxial systems could plummet 46.5% to $17 million. Normal pressure CVD systems will see the most serious decline; that market is expected to drop 62% to $12 million. The market for optical CVDs will be spared any drop.

2M-BIT CMOS MASKED ROM HAS 200-nSEC ACCESS TIME

The Model LH532000 from Sharp Corp is a 2M-bit CMOS masked ROM with a 200-nsec access time that is fabricated using 1.2-μm design rules and a tungsten-silicide process. It comes configured as 256k words×8 bits or 128k words×16 bits. Power consumption is 35 mA. Sample price is ¥2400 ($15.48). Sharp will also offer a 4M-bit CMOS masked ROM, the LH534000, in December. That device will be configured as 512k words×8 bits or 256k words×16 bits, have an access time of 200 nsec, and a power consumption of 50 mA.

Two of a kind!


synthesizer /function generator 0.1mHz-20MHz
PM5192
20MHz
synthesizer /function generator 0.1mHz-50MHz
PM5193
50MHz

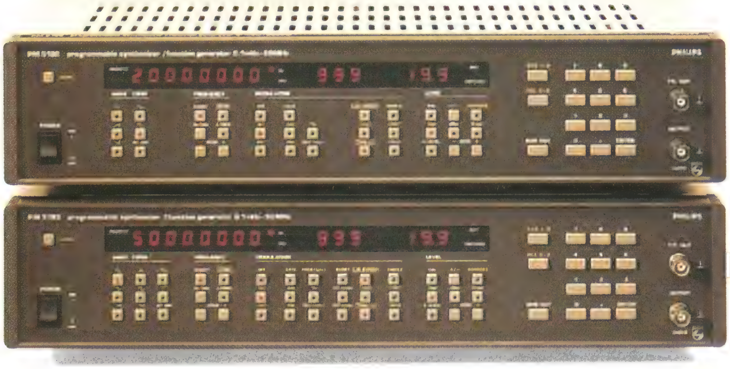
Our PM5192 and PM5193 Synthesizer/Function Generators are two of a kind. Both feature 8-digit frequency resolution; so setting accuracy and reproducibility are guaranteed. Both are IEEE-bus compatible; so they can be integrated into automated system set-ups. Both are housed in identical 19″ cabinets; so they can be placed on a bench or mounted in a rack. And both offer the best value-for-money of any function generator on the market; so you get high performance without having to pay a high price!

■ The PM5192 is a 0.1mHz to 20MHz instrument featuring: 5 selectable waveforms with adjustable output to 20Vpp, and AM/FM/Gating/Lin-Log sweep modulation modes with internal 1KHz modulation frequency. All function buttons have built-in LED status signalling.

■ The PM5193 0.1mHz to 50MHz generator offers the same fine features as the PM5192 plus an extra 3 selectable waveforms (including 3ns-Pulse and Haversine); programmable modulation frequency from 10Hz to 200KHz, and counted burst.

Test the difference

■ Product credibility in technology, technique, quality and service also is assured because the PM5192 and PM5193 Synthesizer/Function Generators are backed by the corporate resources of one of the world's largest electronics companies.



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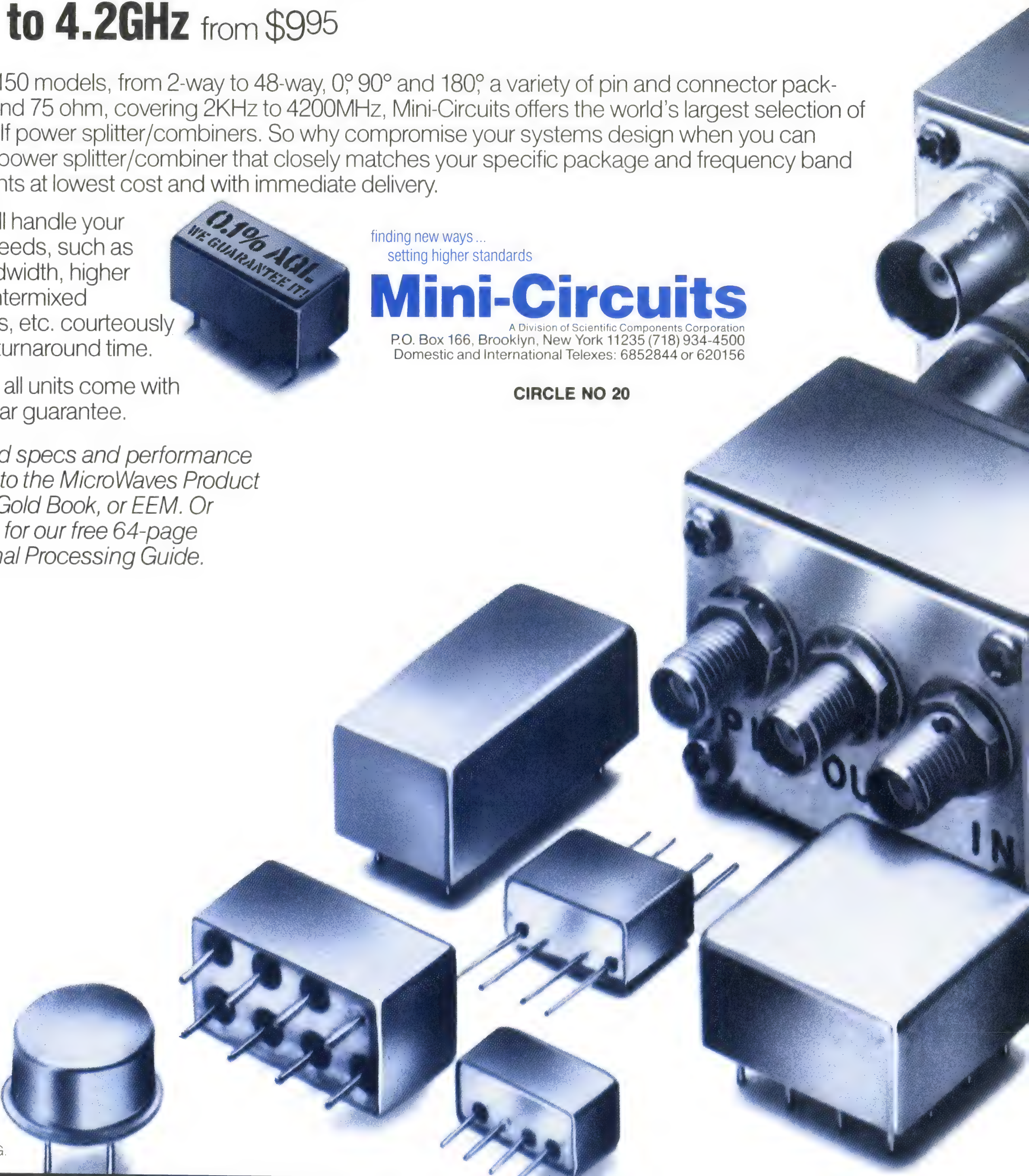

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CIRCLE NO 20

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Discover New World Capabilities.
Our bipolar products offer speed/power programmability at the logic-gate level—to optimize performance and minimize overall power dissipation. In fact, you can get gate delays ranging from 225 to 600 picoseconds, depending upon the level of macro performance desired. With densities of up to 5000 equivalent gates. You can even specify a QM1600S with 1280 bits of static RAM and 1600 logic gates together on one chip.

In addition, our high-density CMOS arrays (up to 10,000 gates) also offer extraordinary performance and efficiency. Typically 1.1ns (while dissipating less than 20μW per gate per MHz). And, if required for your application, all our devices, both bipolar and CMOS, can be processed to MIL-STD-883C Methods.

Something Unexpected On The Horizon.
When you bring us your design ideas, you'll also discover a combination you may not expect. Because in addition to high performance bipolar and CMOS products, we've also brought

per galleon.

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That's exactly the kind of performance capabilities you'd expect from the company that was first to offer a flexible design interface and first to deliver mixed ECL/TTL arrays. Arrays that substantially reduce overall parts count and system power requirements, and simplify component interface.

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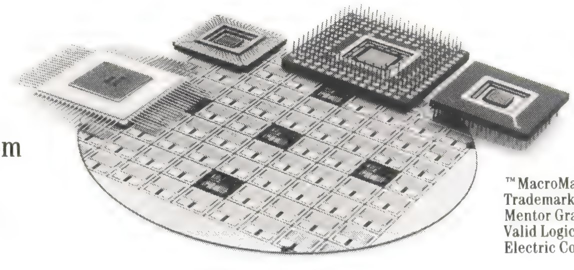

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CIRCLE NO 22

VITELIC INTRODUCES A TRUE CMOS DUAL PORT MEMORY

You used to have only two choices.

If you wanted dual port memory, you could either build it yourself. Or buy the only integrated dual port memory product on the market.

Either way, that wasn't much of a choice. And quite frankly, we kept hearing how much more you wanted.

That's why Vitelic is rolling out an extensive dual port SRAM family. You asked us for a lot more features than what your current options provided.

And you wanted to add these features cost-effectively. Which is why we offer a broad range of parts— from our high-performance V61C32 to our low-cost V61C35.

What about making your designs simpler? No problem. Our dual ports deliver fully asynchronous operation.

You also wanted your system to run faster. So we engineered fast simultaneous access of a common memory from both ports for enhanced throughput.

To guarantee data integrity, we offer on-chip arbitration logic. And for those of you who requested a part for battery backup operation, we feature 2-volt data retention through the use of our exclusive VICMOS full CMOS memory cell approach.

Our CMOS design also provides low power for your battery-operated designs. And extended temperature ranges for applications in harsh environments.

FAMILY	TYPE	PART NO.	DESCRIPTION/ACCESS TIME	AVAIL.
CMOS Dual Port Static RAM Choices	2K x 8	V61C32	Arbitrated, Busy Flag 55/70/90ns	NOW
	2K x 8	V61C35	Multiplexed 55/70/90ns	NOW
	2K x 8	V61C34	Arbitrated, Semaphore 55/70/90ns	1Q87
	2K x 9	V61C37	Arbitrated, Turbomode 30/35/45ns	4Q86
	1K x 8	V61C30	Arbitrated, Interrupt 55/70/90ns	4Q86
CMOS Dual Port Static FIFO Choices	512 x 9	V61C01	Zero Fall-Through Time 25/35/50ns	4Q86
	1K x 9	V61C02	Zero Fall-Through Time 25/35/50ns	4Q86
	1K x 9	V61C03	Zero Fall-Through Time 15/20/25ns	4Q86

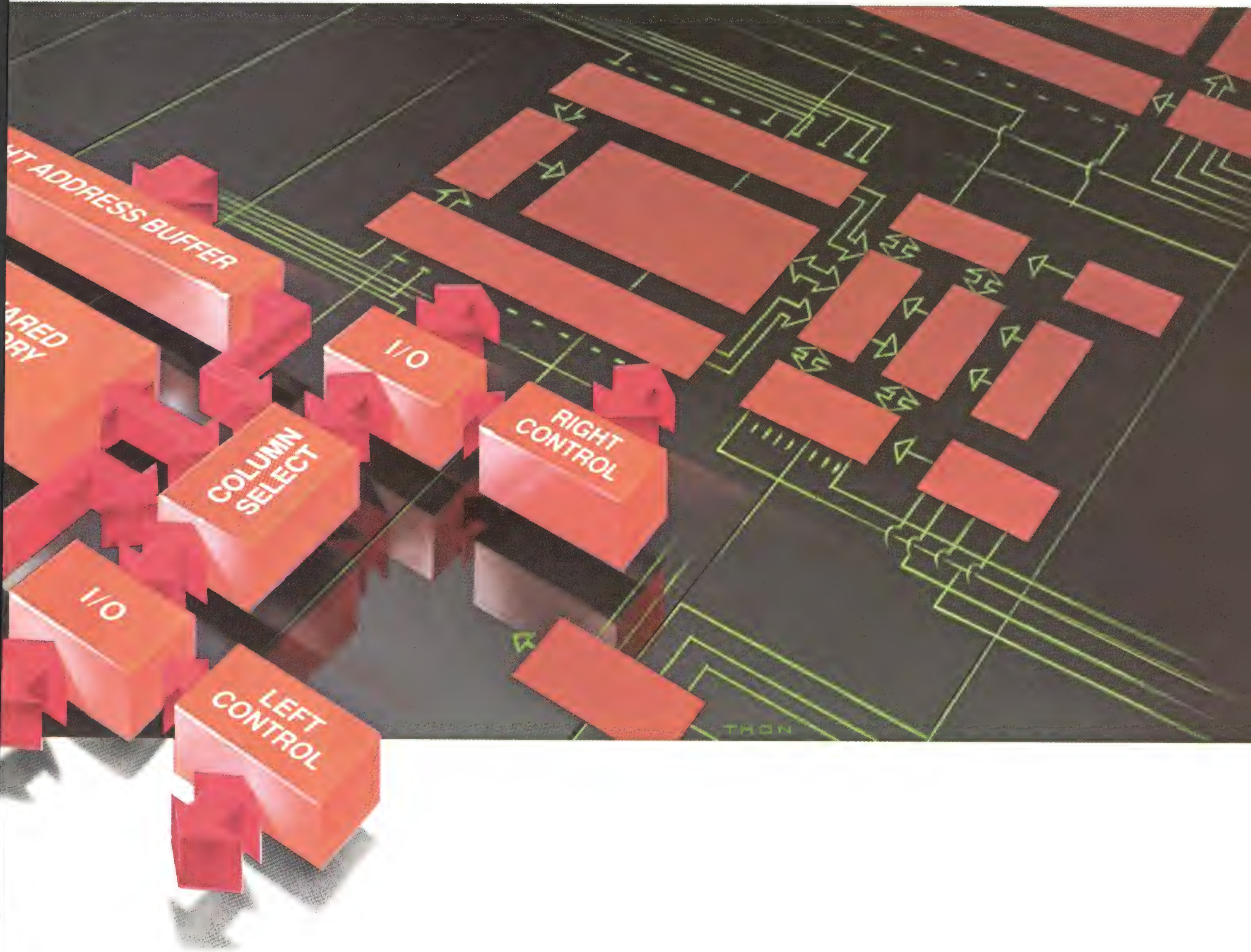
Then you asked for a manufacturer that wouldn't forget about you after the sale. So Vitelic provides ongoing Applications Engineering Assistance to help you build faster, better, and smarter systems.

In addition, we offer a full line of CMOS memory parts. From SRAMs with densities of 16K, 64K, and 256K and speeds as fast as 25ns to CMOS DRAMs with densities of 64K, 256K, and 1M.

And there's a lot more to look forward to from Vitelic. Like our dual port DRAM by the middle of next year. And a family of FIFO later this year.

To find out more about our dual port family or other CMOS memory, just give Vitelic a call at (408) 433-6012. We'll listen to you. Just like we always have.

BREAKTHROUGH IN CHOICE.



VITELIC

Taking The Lead
In Advanced CMOS Memory.

CIRCLE NO 23

NEWS FROM PHILIPS

INTEGRATED CIRCUITS ☐ SEMICONDUCTORS ☐ ELECTRON TUBES ☐ COMPONENTS ☐ ASSEMBLIES ☐ MATERIALS

Breakover diodes protect digital telephone equipment

We are now supplying a series of glass-passivated breakover diodes (BODs) to provide reliable, fast-acting transient over-voltage protection for the latest generation of digital telecommunications equipment. These devices will also help to protect modems, facsimile, telex, and answering machines – as well as data transmission and remote instrumentation monitoring lines.

BODs are designed to operate between 100 V and 280 V and two series are available now: the BR210 series of single bi-directional diodes in a two-terminal TO-220AC outline; the BR220 series of monolithic double-diodes in a TO-220AB outline with three terminals (one common). The monolithic construction of the BR220 ensures that the diodes are evenly matched and exceptionally stable in operation. Other types – designed to meet any special requirements – can be developed as the demand materializes.

BODs go into action within 5 ns of the occurrence of a voltage transient which is within ±12% of their nominal rating. They have a high holding current of >150 mA and can cope with transient peak currents of up to 40 A in an impulse having a rise time of 10 μs and a fall time of 320 μs (equivalent to a 10/700 μs impulse at 1,6 kV as defined by CCITT K17).

BODs will replace voltage-dependent resistors (VDRs) in many applications where they can provide a faster, much more stable and reliable form of protection. They may also replace zener diodes in some applications.

CIRCLE 33

Bit-stream management ICs pair up to ensure fast serial data control rates up to 10 MHz

Philips is announcing two bit-stream management ICs which perform encoding/decoding and serial-parallel conversion in fast serial data controllers at rates of up to 10 MHz. The 8X801 encoder/decoder and the 8X802 serializer/deserializer fit well into any computer system demanding high-speed, reliable data flow.

Used with a microcontroller the pair form a bit-stream manager for disk drives and other computer peripherals, ensuring that the peripherals do not hold up or degrade the performance of the entire system.

The 8X801 works with non-return-to-zero (NRZ) and one of any three transmission coding techniques: frequency modulation for single-density drives; modified frequency modulation (mfm) for double-density drives; and differential Manchester for data communication lines. In the mfm encoding format an internal precompensation circuit generates and detects the encoding violations that serve as address marks. An on-chip phase comparison circuit can be used to build a phase-locked loop for reliable separation of data.

Although ideally for use with the 8X802, the 8X801 is a flexible device which can be used in a variety of design applications. The different encoding formats make it invaluable in designs requiring single- or double-density disk recording, or in data communications applications.

The 8X801, in a 24-pin plastic or hermetic DIL, operates from a +5 V supply. The 8X802, in a 48-pin plastic DIL or in a plastic leaded-chip-carrier, operates from a +7 V supply.

CIRCLE 72

Low-power CMOS versions of 8051 microcontroller family boast selectable reduced activity modes

Now available from Philips are low-power CMOS versions of the industry-standard 8051 8-bit microcontroller. As an official alternate source for Intel Corp., our 8051 and 80C51 families are fully pin- and function-compatible with the Intel devices. The new PCB80C51/PCB80C31 offer the same high-performance functions as previous NMOS versions – such as Boolean processing – while dramatically slashing power requirements.

In addition to a low maximum operating current of just 30 mA, the devices also have two software selectable modes of reduced activity for further power reduction – Idle and Power Down mode. In the Idle mode, maximum current consumption is 10 mA and in the Power Down mode it is only 100 μA. The Idle mode freezes the CPU while allowing the RAM, timers, serial port and interrupt system to continue operating. The Power Down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

The PCB80C51 contains 4 Kbytes of mask-programmable ROM and 128 bytes RAM; the PCB80C31 is a ROM-less version. Both devices feature: 32 I/O lines; two 16-bit timer/event counters; a five-source two-priority nested interrupt structure; a serial I/O port for either multi-processor communication, I/O expansion, or full duplex UART; and on-chip 12 MHz oscillator and timing circuits. For systems that require higher capability, the devices can address up to 64 Kbytes of external program memory and 64 Kbytes of external data memory – a total of 128 Kbytes.

These high-performance microcontrollers are for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and telecommunications. The PCB80C51 is for low-cost, high-volume production and the PCB80C31 for applications requiring the flexibility of external program memory which can be easily modified and updated. Their low power consumption makes them particularly attractive for battery-operated and portable equipment.

CIRCLE 150

PHILIPS

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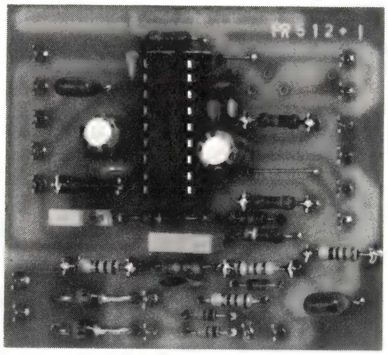
Telephone transmission circuit operates down to very low line voltages



Our newly-introduced TEA1067 telephone transmission circuit is capable of operating from line voltages as low as 1,6 V, thereby facilitating the parallel connection of modern electronic and conventional carbon microphone telephones.

The new circuit features high-impedance (symmetrical 64 kΩ, asymmetrical 32 kΩ) inputs which make it suitable for all current types of dynamic, magnetic, piezoelectric, or electret microphones. The 18-pin device is available in a standard plastic DIL or surface-mounting mini-pack (SO).

The new bipolar circuit performs all the speech and line interface functions required in fully electronic telephone sets. As the TEA1067 integrates many popular features, it enables manufacturers to base a whole range of telephones on just this one circuit. In addition, it meets the performance requirements of most major international PTTs in Europe, the USA, and the Far East.

The TEA1067 is the latest addition to our TEA106X family of versatile telephone circuits with dialler interface. It incorporates all the versatile features of earlier types such as: the possibility to adjust the d.c. line voltage; receiving amplifier for all types of earpieces; mute input for dialling; DTMF transmitter stage; and power down input to guarantee rectangular dial pulse shape on the telephone line.

Apart from the low-voltage operation, another improvement of the TEA1067 is reduced noise of the receiving amplifier which is an advantage for applications with sensitive microphones (electret and piezo). Other features include a voltage regulator with adjustable voltage drop, a supply point with sufficient current to supply low-current CMOS dialler and featurephone ICs, large amplification setting range on microphone and earpiece amplifiers, and a line current dependent automatic gain control adaptable to various exchange supply resistors and voltages.

Normal line current operating range is from 11 to 140 mA; in reduced performance mode the circuit can operate with supply currents down to 1 mA at a line voltage 1,6 V. Maximum operating line voltage is 12 V. Operating ambient temperature range is −25 to +75 °C.

Apart from the TEA1067 the TEA106X family of transmission circuits with dialler interface now consists of: the TEA1060 with low-impedance input for dynamic and magnetic microphones; the TEA1061 with high impedance input for electret and piezo-electric microphones; the TEA1066 in a surface-mounting minipack; the TEA1068 with an input for all types of microphone. Major benefits of the family include the elimination of bulky and costly hybrid transformers and the absence of interface components between the pulse dialler and the speech transmission circuit.

CIRCLE 111

Range of easy-to-use semiconductor lasers with pre-adjusted collimating optics

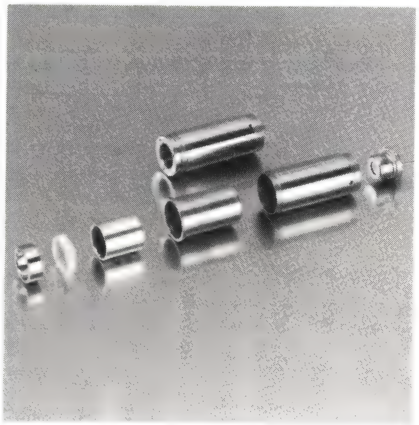
Philips is introducing a range of collimator pens, semiconductor lasers with pre-adjusted collimating optics, which require no specialist knowledge to put into operation. The range currently consists of the 515CQL-A, 515CQL-C, 513CQL-A and CQL16. The collimator pens have comparable emission characteristics to He-Ne gas lasers, but cost far less, are much lighter, require a much lower voltage supply, and are much easier to use. A rugged stainless steel casing – measuring just 27 mm – allows for operation up to 60 °C.

The range is designed for users who are attracted by the features of semiconductor lasers but do not have the know-how to add on collimating optics. The built-in lens system collimates the laser light and corrects for astigmatism to produce a tight, parallel beam with a collimation of less than 0,3 mrad (or 0,3 mm per metre).

The devices are designed primarily for industrial applications such as: optical read or write data recording systems; non-impact printers, bar code readers (supermarket scanners); measurement of distance, speed and surface purity; and theodolites and levellers in the construction industry. Other areas include medical uses, military applications (range finders, proximity switches, target markers), and short distance communication links.

The 513CQL-A offers the highest output power with 20 mW continuous wave. Current consumption with maximum power output at 60 °C is only 250 mA. The wavelength of this laser is 820 nm.

The 515CQL-A, 515CQL-C and CQL16 all have a continuous output power of 2 mW. Current consumption at 60 °C with maximum power output is 150 mA for the 515CQL-A and -C, and 80 mA for the CQL16. Wavelengths are 820, 870 and 780 nm respectively.



CIRCLE 189

PHILIPS

SIGNALS & NOISE

Grammatical goof mars article on writing

Dear Editor:

The Professional Issues article "Learning to write well helps engineers overcome anxieties about communicating" (EDN, July 24, pg 263) quotes Susan Almazol as saying "The reason they have problems is because schools don't teach business writing . . . ." One would expect a teacher of writing to avoid grammatical errors. It would be correct to say "The reason . . . is that schools don't teach business writing . . . " or "They have problems because schools don't teach business writing . . . ." It is incorrect to say "The reason is because . . . ."

Engineers *can* benefit from help in writing, so the article is quite pertinent. And Ms Almazol may indeed be correct in her reservations about word processors. I'm afraid, though, that the grammatical goof spoiled the effect, common though that goof has come to be.

Sincerely yours,
Alfred Skrobisch
The Staver Co
Bay Shore, NY

Readers' comments

- *Sex in ads*

"Congratulations to Rick Nelson for his excellent editorial on sex in advertising ["Getting the (male) engineer's attention," EDN, April 17, pg 51]. However, one editorial is not enough. EDN should refuse advertising that uses that approach. As a male engineer, I look forward to your adoption of such a policy." —*JP, Waltham, MA*

"Your article reflects the feminist view of females; certainly not the real female position, which 4.5 million years of evolution has produced."—*TW, North Wales, PA*

"Rick, thank you for your boldness in speaking out. I myself am offended by seeing skin displayed, but worse still [is] suggestive sexuality. Let the advertisers keep it in their bedrooms and off the circuit board!"—*JG, Patuxent River, MD*

- *Unreal products*

"Regarding the editorial 'It's unreal!' [EDN, May 1, pg 49] . . . this sort of cheap business tactic (and many others) will not cease until corporations rid themselves of the PR and huckster crowd and get back to putting solid business people into the executive ranks. I applaud Mr Legg for his outspoken editorials." —*PB, Atlanta, GA*

- *The money stream*

"Your editorial regarding the

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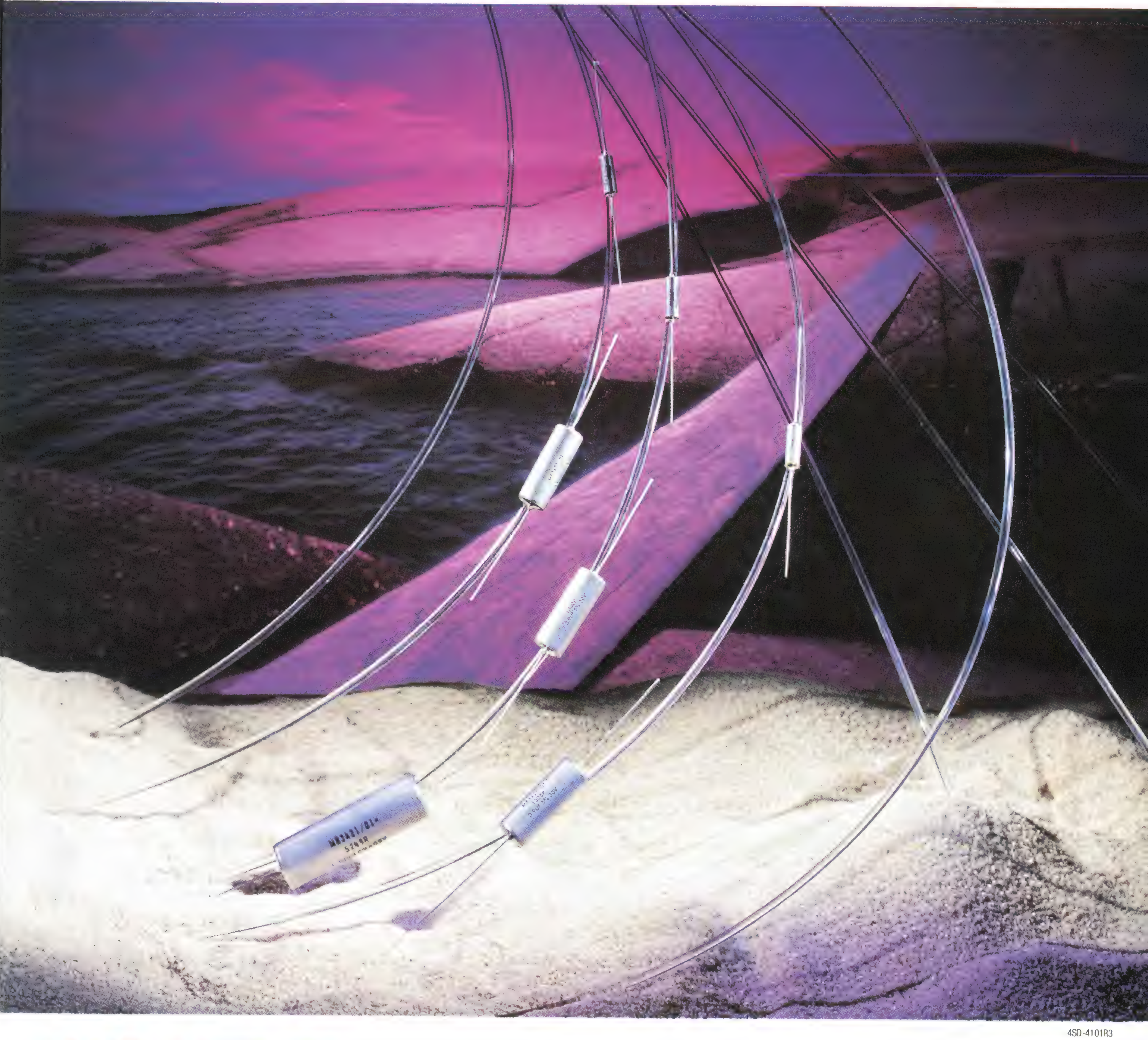
CIRCLE NO 26

1000s OF MISSIONS.



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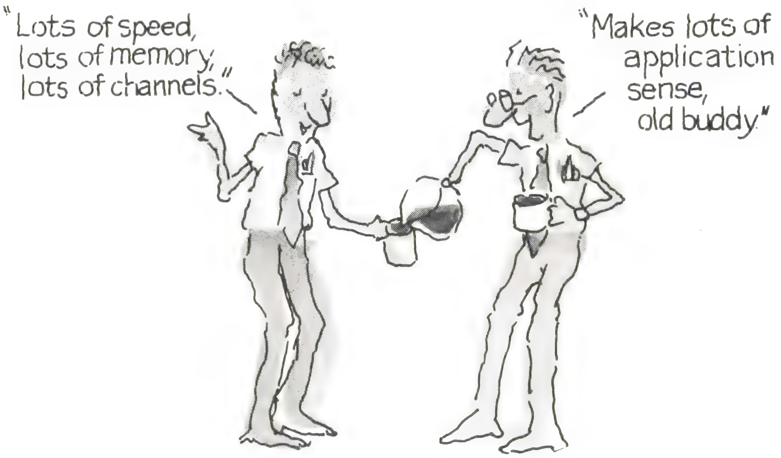
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CIRCLE NO 28

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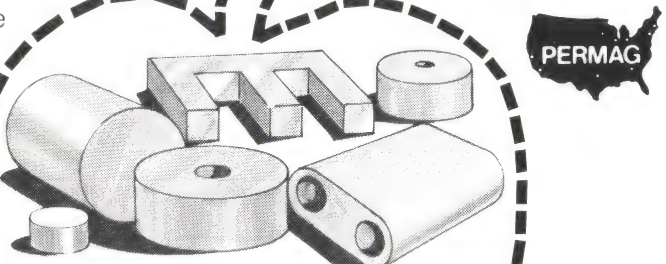

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'money stream' (EDN, June 12, pg 51) is correct and on the mark. I have personal experience in both design and management, where I have found a large financial gap. I am now in the process of returning to management."—*JH, Sudbury, MA*

Corrections

The article "Single-board computers support PC and PC/AT bus" (EDN, July 24, pg 64) lists an incorrect phone number (on pg 73) for Faraday Electronics. The correct number is (408) 749-1900.

The Design Idea entitled "Program computes log magnitude and phase" by Thomas Hack (EDN, August 7, pg 206) contains an error in Listing 2. The line for B(1) should read: B(1)=? 4.153E8. Please note also that the filter's −40.5-dB level of stopband attenuation occurs at 14 kHz.

We regret the omission of RCL Electronics from the listing of manufacturers in the Special Report "Resistor chips, networks, and discrete resistors" (EDN, August 7, pg 140). The company produces industrial- and military-grade wirewound resistors, matched sets, networks, wirewound fuses, temperature sensors, and low-ohm metal-element resistors. You can reach the company at the following address:

RCL Electronics Inc
195 McGregor St
Manchester, NH 03102
(603) 627-3831
Circle No 600

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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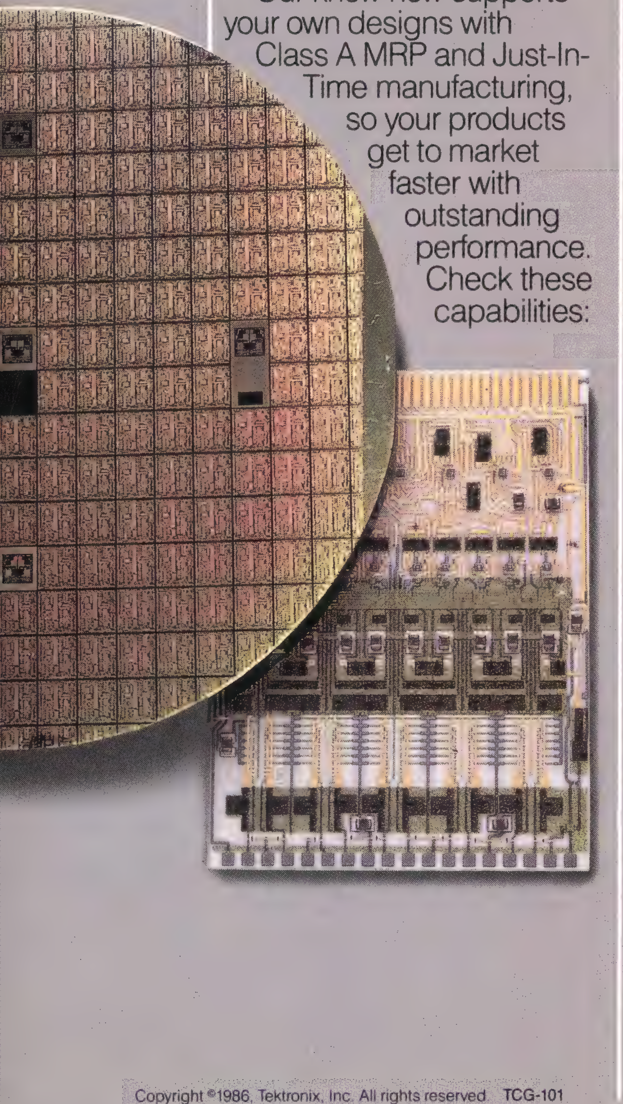

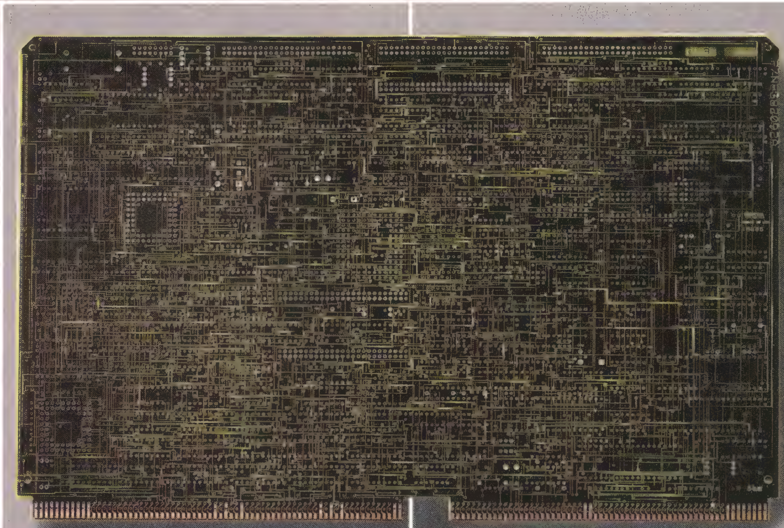

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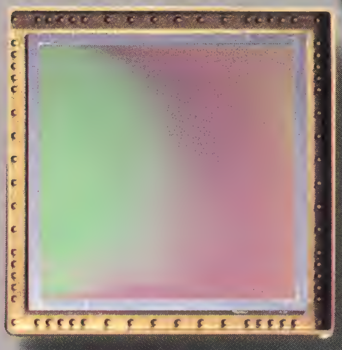

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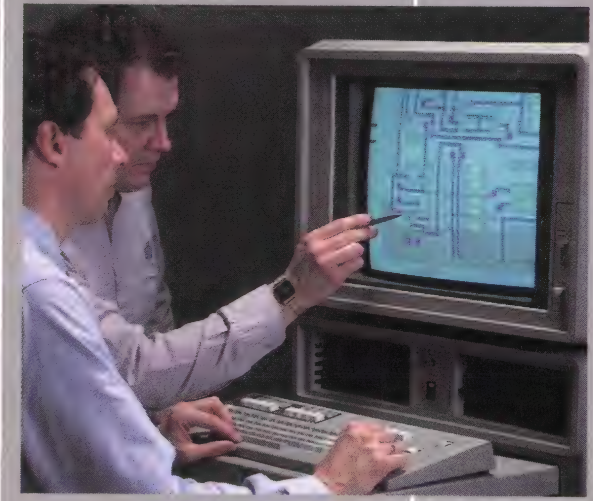

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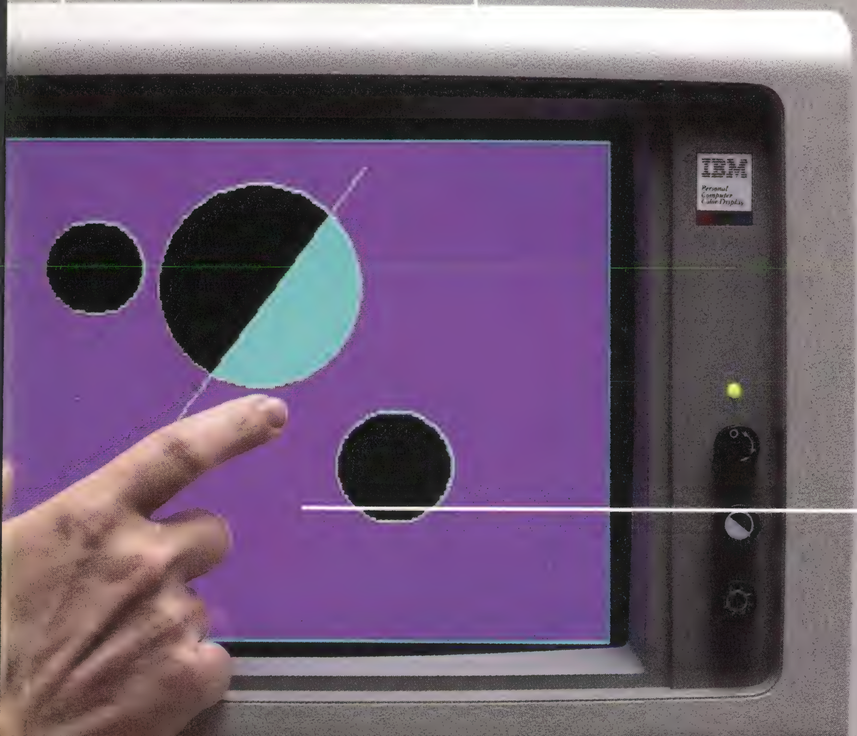

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CIRCLE NO 29

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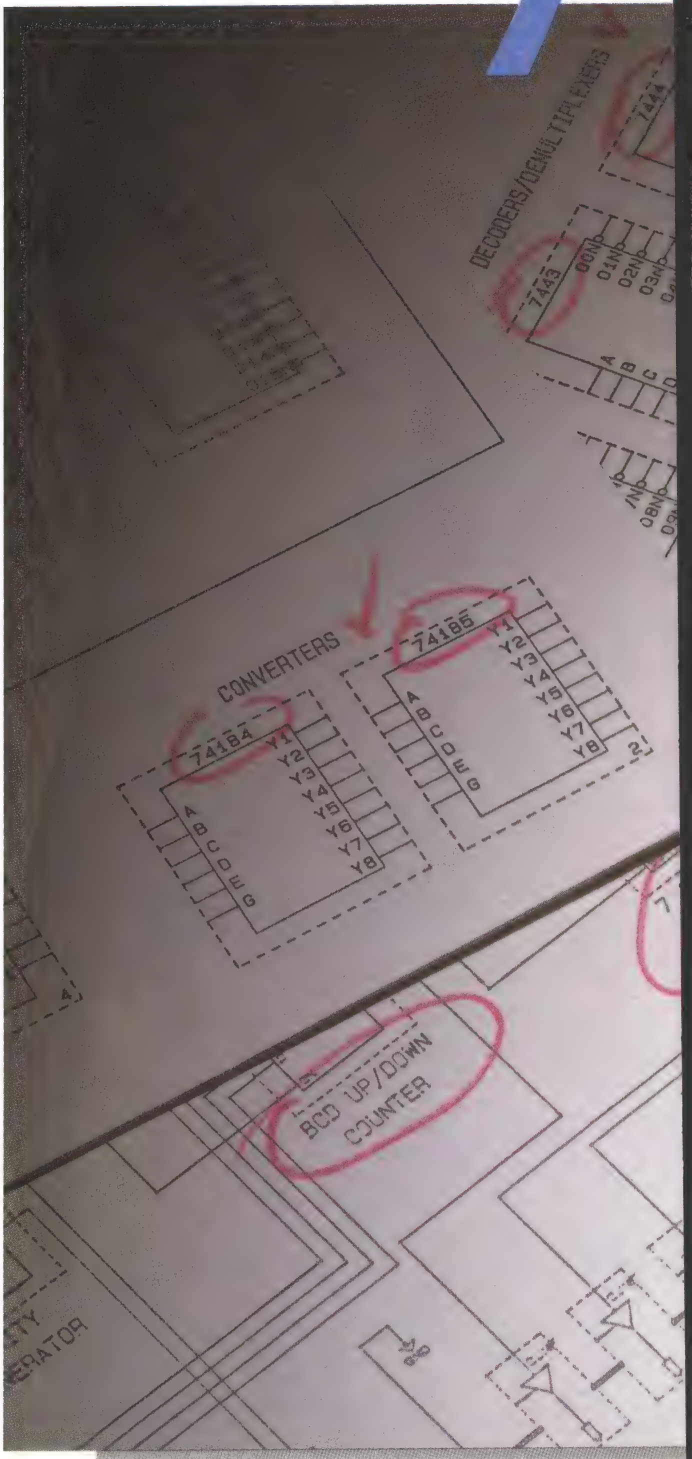

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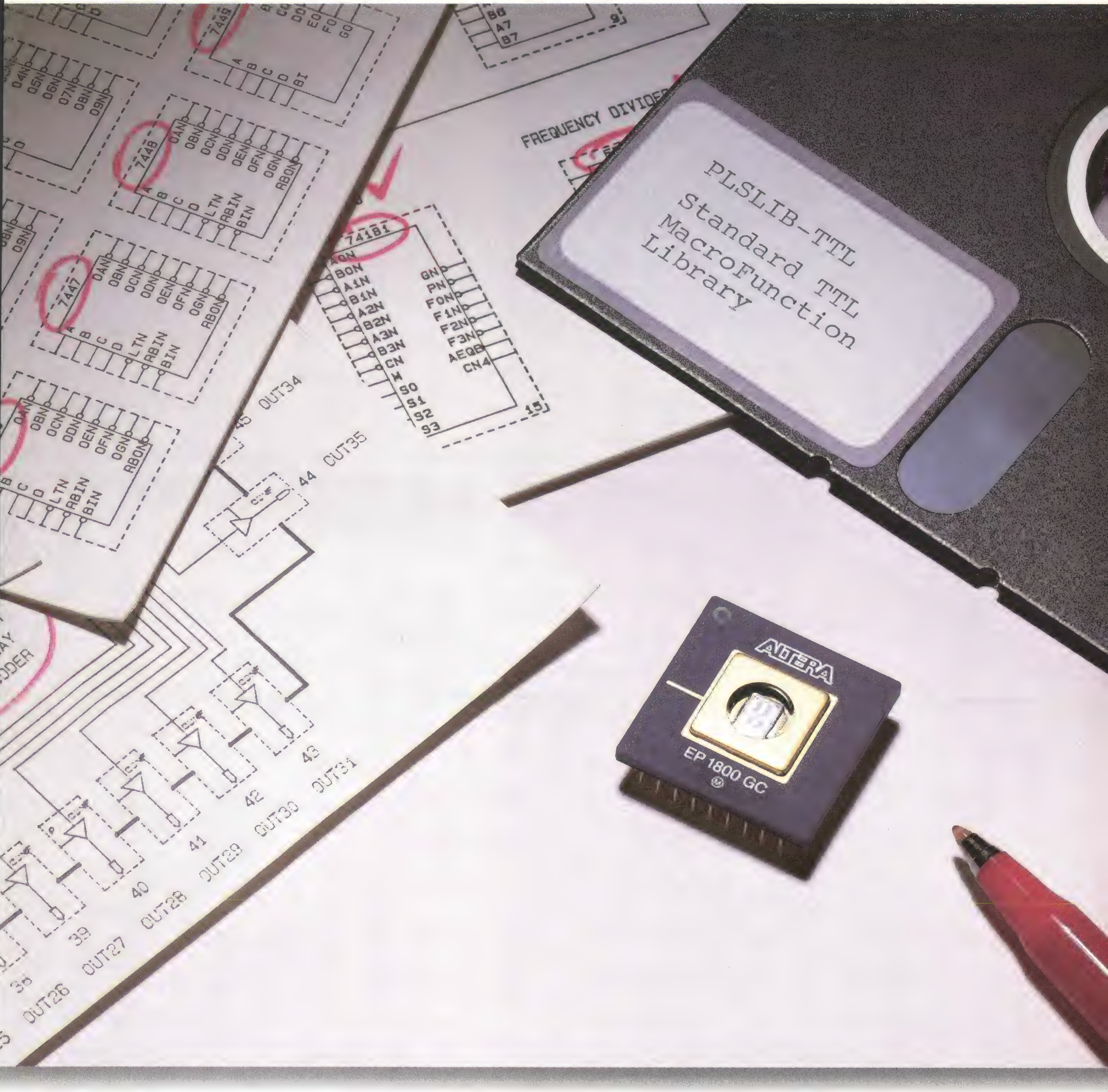

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PMI AMP-05	100	50pA	10*	15*	No	No
AD AD524	100	15,000pA	15	—	Yes	Yes

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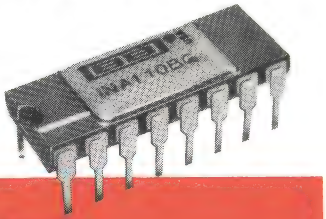

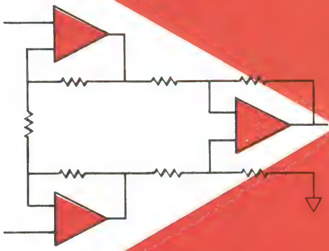

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CALENDAR

International Conference of the iRMX Operating System Users Group, Portland, OR. Catherine Moon, Intel Corp, HF2-60, 5200 NE Elam Young Parkway, Hillsboro, OR 97124. (503) 640-7038. October 27 to 28.

Pacific Northwest Computer Graphics Conference, Eugene, OR. Conference Manager, University of Oregon Continuation Ctr, 1553 Moss St, Eugene, OR 97403. (800) 228-6891; in OR, (800) 824-2714. October 27 to 28.

Advanced Signal Processing (short course), Inglewood, CA. Evolving Technology Institute, 3725 Talbot St, Suite F, San Diego, CA 92106. (619) 224-3788. October 27 to 29.

IEEE Holm Conference on Electrical Contacts, Boston, MA. IEEE Components, Hybrids, and Manufacturing Technology Society, 345 E 47th St, New York, NY 10017. (212) 705-7405. October 27 to 29.

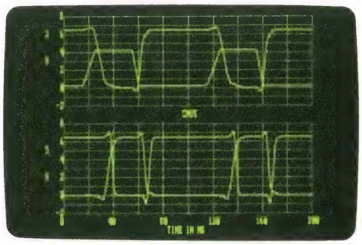
Interface International, Paris, France. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. In Europe, contact World Trade Ctr, Tower C, 12th fl, Strawinskylaan 1245, 1077xx Amsterdam, The Netherlands; (31) 20-621941. October 27 to 29.

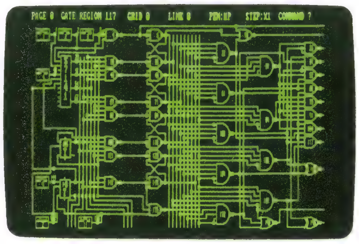
ATE Silicon Valley, Santa Clara, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 27 to 30.

Satech '86 (Systems Automation Technologies Conference and Exhibition), Boston, MA. Intertec Communications, 2472 Eastman Ave, Bldg 34, Ventura, CA 93003. (805) 658-0933. October 27 to 30.

Systec '86 (International Trade Fair for Computer Integration), Munich, West Germany. Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07540. (201) 652-7070. October 27 to 30.

MICRO CAP and MICRO LOGIC put your engineers on line... not in line.


"Typical MICROCAP Transient Analysis"


"Typical MICROLOGIC Diagram"

How many long unproductive hours have you spent "in line" for your simulation? Well, no more. MICROCAP and MICROLOGIC can put you on line by turning your PC into a productive and cost-effective engineering workstation.

Both of these sophisticated engineering tools provide you with quick and efficient solutions to your simulation problems. And here's how.

MICROCAP: Your Analog Solution

MICROCAP is an interactive analog circuit drawing and simulation system. It allows you to sketch a circuit diagram right on the CRT screen, then run an AC, DC, or Transient analysis. While providing you with libraries for defined models of bipolar and MOS devices, Opamps, transformers, diodes, and much more, MICROCAP also includes features not even found in SPICE.

MICROCAP II lets you be even more productive. As an advanced version, it employs sparse matrix techniques for faster simulation speed and larger networks. In addition, you get even more advanced device models, worst case capabilities, temperature stepping, Fourier analysis, and macro capability.

MICROLOGIC: Your Digital Solution

MICROLOGIC provides you with a similar interactive drawing and analysis environment for digital work. Using standard PC hardware, you can create logic diagrams of up to 9 pages with each containing up to 200 gates. The system automatically creates the netlist required for a timing simulation and will handle networks of up to 1800 gates. It provides you with libraries for 36 user-defined basic gate types, 36 data channels of 256 bits each, 10 user-defined clock waveforms, and up to 50 macros in each network. MICROLOGIC produces high-resolution timing diagrams showing selected waveforms and associated delays, glitches, and spikes—just like the real thing.

Reviewers Love These Solutions

Regarding MICROCAP . . . "A highly recommended analog design program" (PC Tech Journal 3/84). "A valuable tool for circuit designers" (Personal Software Magazine 11/83).

Regarding MICROLOGIC . . . "An efficient design system that does what it is supposed to do at a reasonable price" (Byte 4/84).

MICROCAP and MICROLOGIC are available for the Apple II (64k), IBM PC (128k), and HP-150 computers and priced at $475 and $450 respectively. Demo versions are available for $75.

MICROCAP II is available for the Macintosh, IBM PC (256k), and HP-150 systems and is priced at $895. Demo versions are available for $100.

Demo prices are credited to the purchase price of the actual system.

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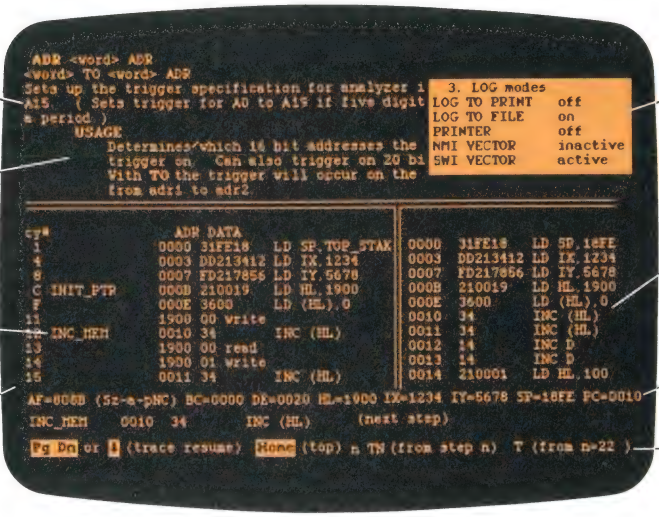
CIRCLE NO 32

Microprocessor Development Dreams Come True!



```
ADR <word> ADR
<word> TO <word> ADR
Sets up the trigger specification for analyzer i   3. LOG modes
A15  ( Sets trigger for A0 to A19 if five digit LOG TO PRINT   off
a period )                                       LOG TO FILE    on
      USAGE                                      PRINTER        off
         Determines which 16 bit addresses the   NMI VECTOR     inactive
         trigger on.  Can also trigger on 20 bi  SWI VECTOR     active
         With TO the trigger will occur on the
         from adr1 to adr2
─────────────────────────────────────────────────────────────────────────
cy#               ADR DATA                      │ 0000  31FE18   LD SP,18FE
 1                0000 31FE18   LD SP,TOP_STAK  │ 0003  DD213412 LD IX,1234
 4                0003 DD213412 LD IX,1234      │ 0007  FD217856 LD IY,5678
 8                0007 FD217856 LD IY,5678      │ 000B  210019   LD HL,1900
 C INIT_PTR       000B 210019   LD HL,1900      │ 000E  3600     LD (HL),0
 F                000E 3600     LD (HL),0       │ 0010  34       INC (HL)
11                1900 00 write                 │ 0011  34       INC (HL)
12 INC_MEM        0010 34       INC (HL)        │ 0012  14       INC D
13                1900 00 read                  │ 0013  14       INC D
14                1900 01 write                 │ 0014  210001   LD HL,100
15                0011 34       INC (HL)        │
AF=000B (Sz-a-pNC) BC=0000 DE=0020 HL=1900 IX=1234 IY=5678 SP=18FE PC=0010
INC_MEM    0010  34         INC (HL)          (next step)
Pg Dn or ↓ (trace resume)  Home (top) n TN (from step n)  T (from n-22 )
```

On-Line Help menus, Command Glossary, and Word List.

Windows can be used to view source files, previous traces, and more.

Symbol translation or source code line display.

Screen displays scroll off into history buffer – can be viewed later.

Pop-up Mode Selection panel called by soft key.

Disassembly of code in memory can be compared with trace in adjacent window.

Symbolic debug register display.

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If you set a breakpoint and single-step, you can then go back to using the analyzer without missing a beat. You can even execute a DOS batch file from UniLab to edit, assemble, and link, then automatically load the new program and symbol table. UniLab uses the full power of the PC.

Find bugs fast with Hardware-assisted Debugging

The traditional way to look for bugs is to single-step through suspect parts of the code until you catch it in the act. This requires a lot of guessing and wasting time.

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UniLab lets you use commands or menus – or a mixture of both. An on-line manual, soft-key help screens, a glossary of commands and their parameters, with full-screen writeups are also at the ready.

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CIRCLE NO 35

CALENDAR

Digital Signal Processing, Single-Chip DSP and Parallel Processors—Theory, Design, and Applications (short course), Dallas, TX. DSP Associates, 18 Peregrine Rd, Newton, MA 02159. (617) 964-3817. October 27 to 31.

Maecon (Mid-America Electronics Conference), St Louis, MO. (313) 254-5310. October 28 to 29.

Southwest Semiconductor and Electronics Exposition, Phoenix, AZ. Cartlidge & Associates, 1101 S Winchester Blvd, Suite M259, San Jose, CA 95128. (408) 554-6644. October 28 to 29.

Simulation and Computer Graphics: Design Tools for Effective Robot Applications (seminar), Norcross, GA. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. October 28 to 30.

Real-Time Operating Systems: A Hands-On Workshop, Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. October 28 to 31.

Electronics India '86, Bombay, India. Industrial and Trade Fairs International, Oriel House, 26 the Quadrant, Richmond, Surrey, TW9 1DL, UK. 01-940-6065. October 29 to 31.

Northeast Computer Faire, Boston, MA. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. October 30 to November 1.

Process Control and Instrumentation India '86, Bombay, India. Industrial and Trade Fairs International, Oriel House, 26 the Quadrant, Richmond, Surrey, TW9 1DL, UK. 01-940-6065. November 1 to 3.

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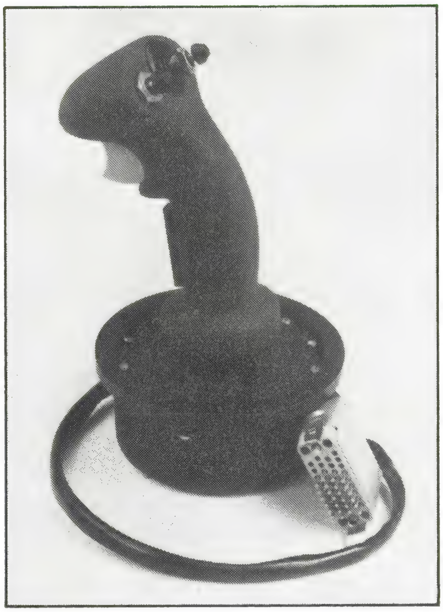

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MC68020 vs. 80386.

How to run apples-to-apples vs. apples-to-oranges benchmarks on these archrival 32-bit MPUs.

WHETSTONE PERFORMANCE

The Whetstone is a standard double-precision, floating-point benchmark written in FORTRAN.

MC68020/68881	80386/80387
• Execution of standard Whetstone benchmark written in FORTRAN: recognized and run by all leading systems manufacturers (Cray, DEC, IBM, etc.).	• Execution of vendor-modified Whetstone benchmark written in C: nobody else in the industry uses this particular procedure.
• Double-precision floating point: specified by standard Whetstone for high accuracy.	• Single-precision floating point: non-standard Whetstone sacrifices accuracy for "performance."
• Complete, 10-loop-count execution: 1 million Whetstone instructions.	• Incomplete, 2-loop-count execution: only 200,000 Whetstone instructions.
• Unary instructions executed: specified by standard Whetstone; single-operand operations.	• No unary instructions executed: intentional '386-vendor modifications to Whetstone spec avoids single-operand operations.
• Entire Whetstone benchmark procedure was not modified from the original standard: no tricks or tweaks to hype performance.	• Altered Whetstone benchmark procedure allowed '386 vendor more favorable results: avoided branch control overhead.
Result: 1.24 million Whetstones/second with commercially-available silicon (68020, 68881).	**Result:** Claims that have no apples-to-apples comparison to reality.

DHRYSTONE PERFORMANCE

The Dhrystone Benchmark measures CPU performance on a typical mix of high-level language statements.

MC68020	80386
• Dhrystone results measured on commercially-available system: Sun Microsystems 3/200 workstation.	• Dhrystone results measured on specially-modified "hot box" built by '386 vendor: '386 "starter kit" version not commercially available.
• Commercially-available operating system (UNIX®).	• No operating system used: '386 vendor used own modified debug monitor.
• Commercially-available UNIX® C compiler (cc).	• '386 Vendor used own internal "beta" version of C compiler: not commercially available.
• Real-world memory architecture: Dhrystone WRITE operations must pass through to main-memory DRAM.	• Utopian memory architecture: zero-wait-state WRITE operations to unlimited cache SRAM—no write through to main memory.
Result: 6362 Dhrystones with commercially-available, real-world systems.	**Result:** Claims that have no apples-to-apples comparison to reality.

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Choosing the world's highest-performance 32-bit microprocessor should be as easy as making an apples-to-apples comparison with such industry-standard benchmarks as Whetstone and Dhrystone performance.

How to tell apples from oranges.

When pulling an apples-to-apples comparison, anyone, anywhere, should be able to easily duplicate the comparison factors and results.

Repeatably.

Attempt no. 1.

So, when comparing the MC68020 and 80386, the first task is to find one of each to compare.

Motorola expects to ship over a quarter of a million MC68020s this year, so finding one of them shouldn't be too difficult. Get the fastest available—a 25 MHz—and a 20 MHz Motorola floating-point coprocessor, the MC68881.

Next (things get a little harder here), try to get your hands on a fully functional, bug free 80386 MPU and 80387 floating point.

And now you know why it's so hard to make an apples-to-apples comparison: you can get the Motorola devices, but "comparable" '386 and '387s? No way. You have to settle for the slower '386 and the promise of silicon yet to come on the '387.

Attempt no. 2.

All right, if you cannot find the chips, reach for readily-available 32-bit systems and compare real, live, '020- and '386-based systems from the open, commercial market.

Exasperating, isn't it? There are hundreds of choices of commercially-available, '020-based systems. But, finding comparable '386-based systems…?

Attempt no. 3.

Running real benchmarks on real products is the best comparison. There have been two attempts at questionable comparisons. Now it's time to try some industry-standard approaches, such as Whetstone and Dhrystone benchmarking. That should allow an apples-to-apples comparison, shouldn't it? If not, at least an apples-to-apples "paper" comparison should be used.

Shown here are currently-available Whetstone and Dhrystone procedures for the MC68020 and the 80386 32-bit processors. Should you wish to use industry-standard methods of comparison, you'll have to—must—rerun the Whetstones and Dhrystones for the '386 along the same universally-accepted lines as for the '020.

And discover which processors have the greater potential for being keystones and which for being millstones in your new designs. The MC68020 is *still* the highest-performance microprocessor no matter how you slice it!

For more information on the world's highest-performance 32-bit microprocessor, the MC68020, fill out the coupon and mail it to Motorola.

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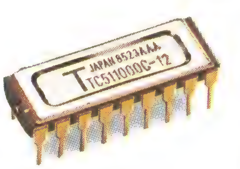

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TC511000 - 12	1 Mb x 1	CMOS	120 ns	Fast Page	18 pin
TC511001 - 10	1 Mb x 1	CMOS	100 ns	Nibble	18 pin
TC511001 - 12	1 Mb x 1	CMOS	120 ns	Nibble	18 pin
TC511002 - 10	1 Mb x 1	CMOS	100 ns	Static Column	18 pin
TC511002 - 12	1 Mb x 1	CMOS	120 ns	Static Column	18 pin
TC514256 - 10	256K x 4	CMOS	100 ns	Fast Page	20 pin
TC514256 - 12	256K x 4	CMOS	120 ns	Fast Page	20 pin
TC514258 - 10	256K x 4	CMOS	100 ns	Static Column	20 pin
TC514258 - 12	256K x 4	CMOS	120 ns	Static Column	20 pin

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TC55257 - 12	32K x 8	CMOS	120 ns	1mA MAX	28 pin
TC55257L - 10	32K x 8	CMOS	100 ns	100μA MAX	28 pin
TC55257L - 12	32K x 8	CMOS	120 ns	100μA MAX	28 pin

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CIRCLE NO 36

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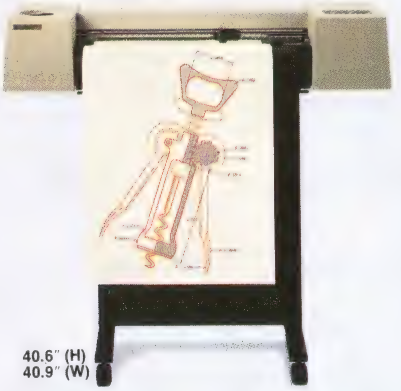
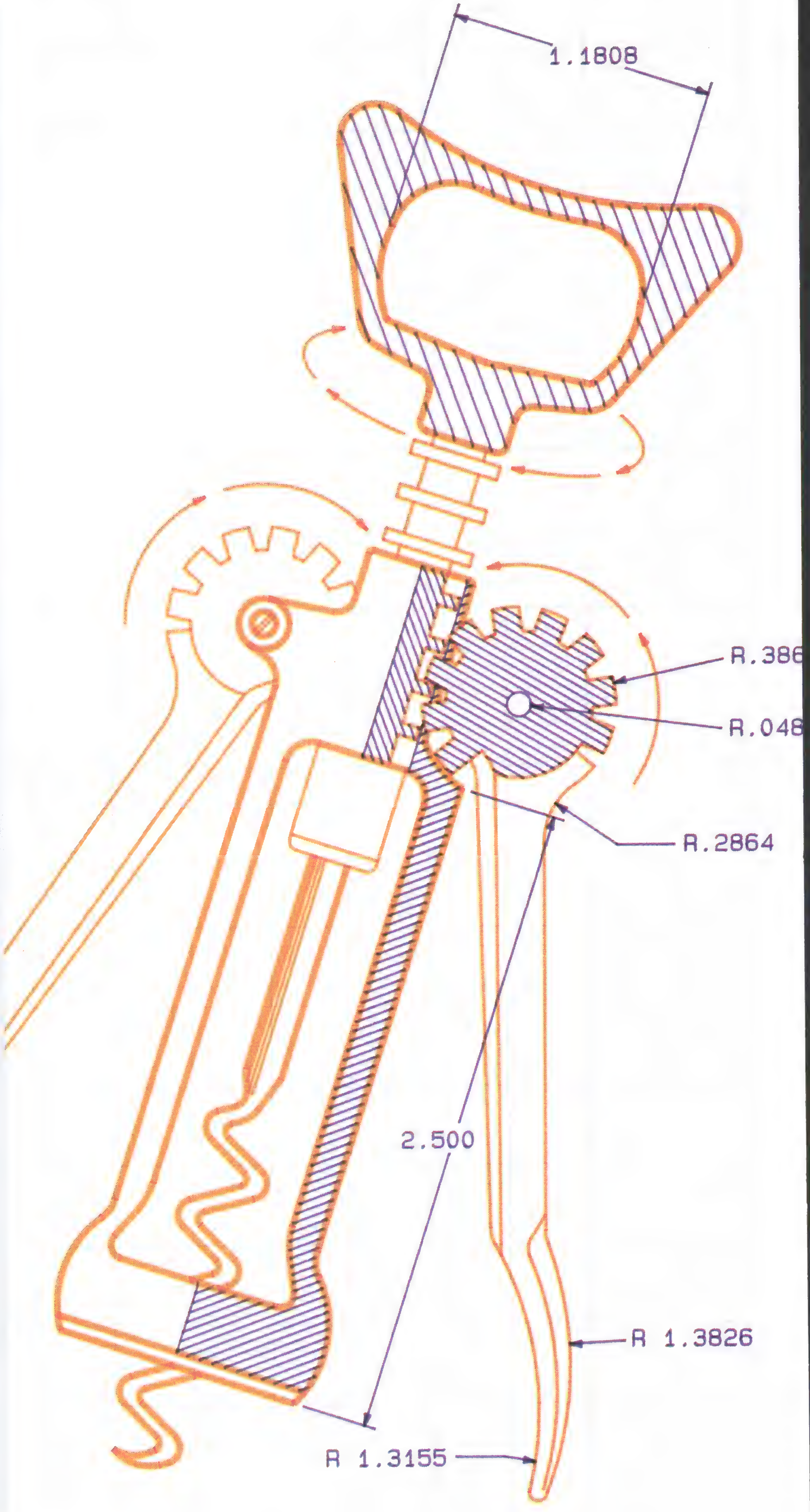


This diagram is an unretouched reproduction of a drawing produced on the HP DraftPro with VersaCAD software.

HEWLETT PACKARD



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CIRCLE NO 37

EDITORIAL

Don't yield to computer-aided thinking

I always feel uneasy when I read about computer programs that purport to locate usage errors, pinpoint excessive use of the passive voice, and perform other editing tasks. My unease stems in part from friends' warnings that predict my imminent replacement by these so-called "intelligent" grammar- and style-checking programs.

But my unease seems disproportionate to the lack of seriousness with which I take those comments. After all, writing is infinitely perfectable; I can spend time turning barely adequate manuscripts into good ones, or good ones (presumably, those that have already been enhanced by a grammar- and style-checking program) into excellent ones. Indeed, the latter job should be more rewarding, so why can't I welcome these programs as readily as, for example, Fortran for engineering calculations, spreadsheets for budgeting, word processors for writing, and CAE programs for circuit design and layout? Why shouldn't such programs be of particular use to EDN's readers and editors alike, many of whom have sidestepped extensive training in writing in favor of engineering, math, and physics?

The answers to these questions lie in the reasons for using various types of programs. Fortran, word processors, spreadsheets, CAE programs, and even spelling checkers essentially speed operations that a user already knows how to perform, and those programs yield a result that's readily verifiable: The numerical answer is either correct or it isn't; the circuit either meets its spec or it doesn't; the word is either spelled correctly or it isn't.

In contrast, the grammar and style checker is nothing but an ineffectual attempt to bring to writing a quality that can only come from years of study and practice. Moreover, these programs lack the authority that other types of programs can demonstrate. For example, a CAE package that consistently fails to design circuits that meet spec wouldn't find a market; in contrast, users might incorrectly suppose that their writing is adequate on the basis of a style checker's poorly defined "readability," "strength," "descriptive," and "jargon" indexes. Yet a checker's ability to point out instances of the passive voice falls far short of the ability to detect a false scent, an ambiguity, or a diversion from thematic continuity.

This lack of authority is a problem that could be overcome as artificial-intelligence techniques mature. Imagine, for example, a program that embodied the knowledge of Strunk and White's *The Elements of Style* and that could produce a critique that might have been written by E B White himself. Now, however, the grammar and style checkers are at best toys that uncover the types of errors that a good writer would never make in the first place. At worst, the programs are crutches that allow users to limp through writing projects that they should never have undertaken. In other words, for many users, minimum standards of good writing could become maximum standards. The problem with such programs suggests the kind of problems that will accompany the design of artificial-intelligence systems if real intelligence isn't brought to bear at the outset.

Rick Nelson

Rick Nelson
Managing Editor

Anti-aliasing enhances measurement confidence. Signal distortion (sample mode only) is shown at high frequencies (top). The peak detect mode displays peak information without signal distortion (bottom).

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INTRODUCING TWO DIGITAL STORAGE SCOPES WITH SOME MIGHTY IMPRESSIVE NUMBERS.

Features	2230	2220
Analog/Digital Storage Bandwidth	100 MHz	60 MHz
Single Shot (Transient) B.W. (10 points per signal period)	2 MHz	2 MHz
Maximum Sampling Speed	20 MS/s	20 MS/s
Record Length	4K/1K (selectable)	4K
Save Reference Memory	One, 4K Three, 1K	One, 4K
Vertical Resolution	8 bit 10 bit (avg mode)	8 bit
Peak Detect	Yes (100 ns)	Yes (100 ns)
Averaging	Yes (menu-selectable)	Yes (rep. sampling)
X-Y Storage Bandwidth	100 MHz	60 MHz
GPIB/RS-232-C Options	Yes (talker/listener, includes 26K of battery-backed memory)	Yes (talker/listener)
Price	$5150	$4150

From 4K record length to 20 MS/s sampling at 100 MHz or 60 MHz... our two new scopes have just what you're looking for! The 2230 and 2220 are powerful digital storage oscilloscopes—and the first scopes in their class that include non-storage capability to these bandwidths.

You can reference, compare, and analyze waveforms with digital storage convenience, plus the confidence you get with analog measurements. Simply switch to the non-store mode to view the signal that the scope has digitized. Only Tek offers this flexibility to 100 MHz and 60 MHz in affordable scopes.

Enhancing use of the scopes as design and troubleshooting tools are fast sample and hold detector circuits, plus the proprietary peak detect mode. They enable the display of pulses as narrow as 100 ns at any sweep speed—even on a single sweep.

You'll also find such features as post-acquisition expansion and compression, X-Y capability to each scope's storage bandwidth and, for systems use, optional GPIB or RS-232-C interfaces.

Best of all, the 2220 and 2230 are easy to use and afford. And backed by Tek's famous 3-year warranty that includes the CRT. Check the front panels. The controls are familiar, comfortable, easy to identify. Designed to push productivity and minimize training time.

In the 2230, CRT readout of front panel settings and key parameters means even more convenience, with cursors for waveform voltage and timing measurements.

Get the reliability and performance you expect in Tek scopes, now enhanced by digital storage, at unexpected prices: $4150 for the 2220, $5150 for the 2230.

For the full story, and more impressive numbers, contact your local Tek Sales Representative today. Or call the Tek National Marketing Center,

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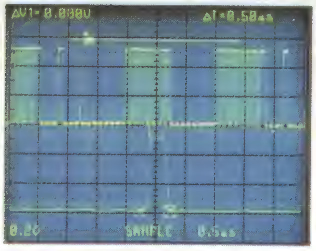
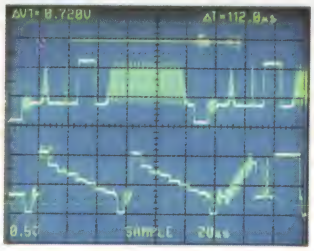
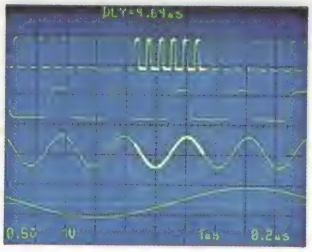


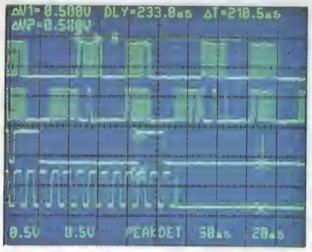
On-screen viewability lets you expand, compress, and position waveforms saved in reference memory. This permits easy viewing and display flexibility of up to eight saved waveforms.



High display resolution and accuracy permits on-screen viewing of signals such as the TV test signal shown here. 4K of record information can be viewed in 1K windows.



100 MHz, non-storage capability comes standard in the 2230. In addition, there's dual channel, dual timebase, versatile triggering and CRT readout.



The 2230 offers the convenience of CRT readout in both storage and non-storage modes at 100 MHz. Storage mode cursors make ΔV, ΔT, and 1/ΔT measurements fast and easy.

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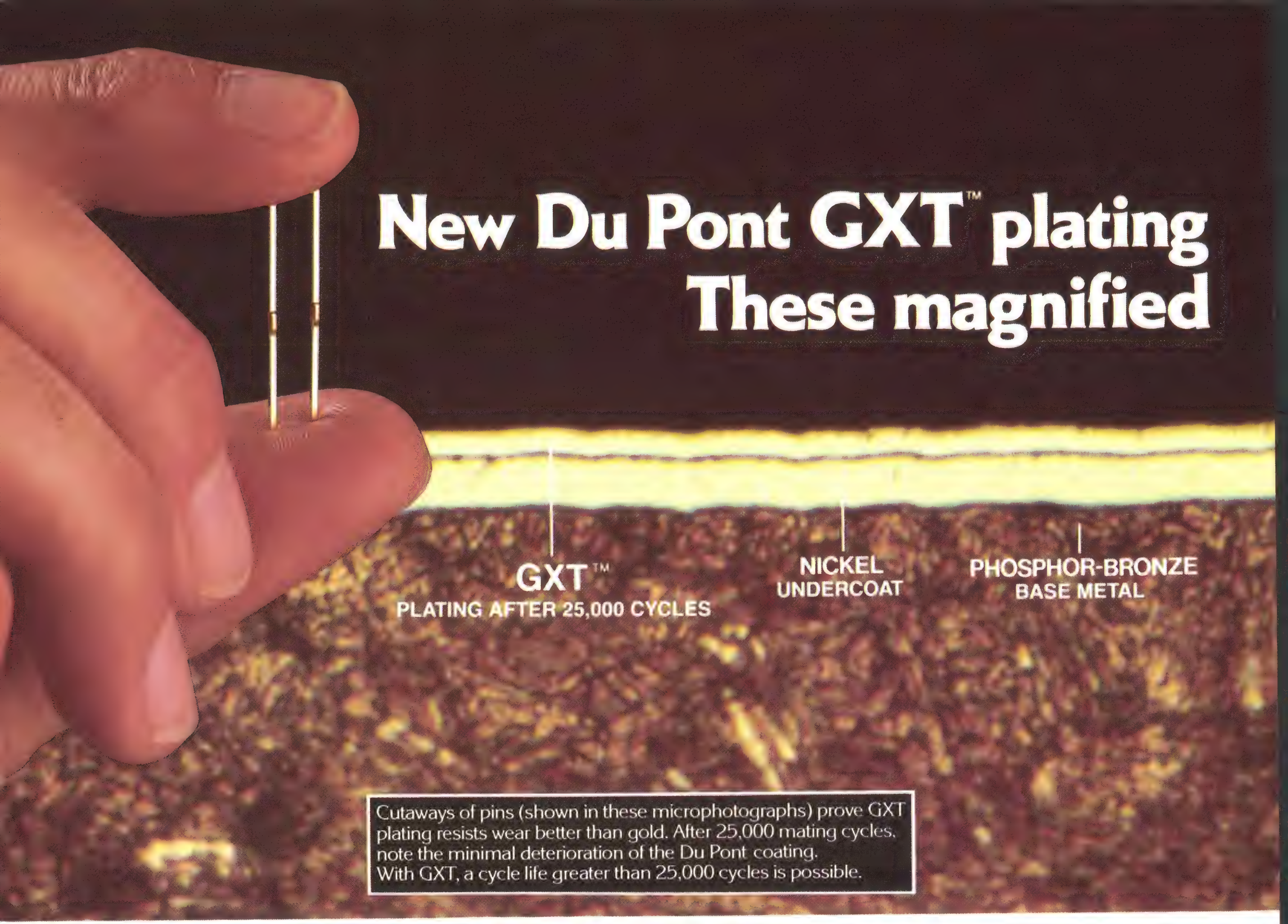
CIRCLE NO 38

New Du Pont GXT™ plating These magnified

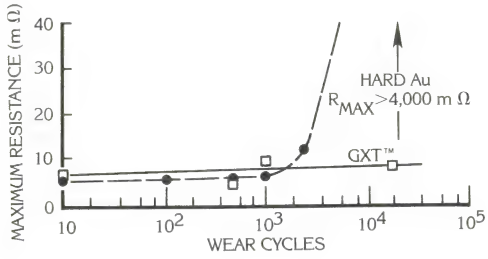


Cutaways of pins (shown in these microphotographs) prove GXT plating resists wear better than gold. After 25,000 mating cycles, note the minimal deterioration of the Du Pont coating. With GXT, a cycle life greater than 25,000 cycles is possible.

Tests also show the GXT plating system is better than gold in solderability, porosity, bend ductility, and corrosion resistance. Yet GXT can reduce costs as much as 20%.

Independent testing laboratories have proved that the Du Pont GXT plating system is *superior to gold* in wear resistance, solderability, porosity, environmental corrosion resistance and bend ductility. And is as *good as gold* in contact resistance and wire-wrapping performance.

Moreover, connectors protected by this remarkable new coating system frequently cost considerably less than comparable parts plated with gold. For example, savings of up to 20% are possible on pins plated with GXT. (Savings depend on the price of gold and upon the amount of gold being replaced.)



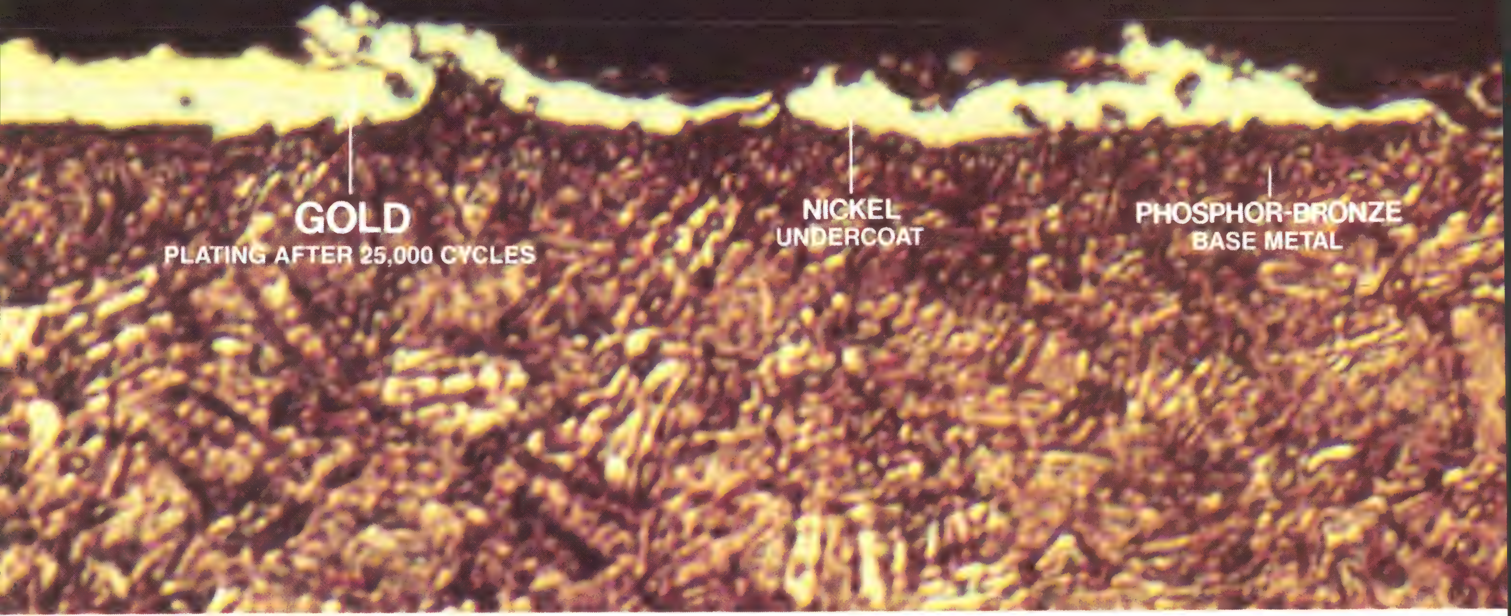
GXT assures minimum contact resistance after wear and exposure to H_2S

By 25,000 cycles, gold shows contact resistance increases to 4,000 milliohms or higher. In contrast, GXT shows excellent electrical performance even after 25,000 cycles.

GXT is a trademark of the Du Pont Company.

Berg Electronics is now

outwears, outperforms gold. connector pins prove it.



In these tests, other gold substitutes didn't measure up to GXT, either. In porosity, solderability, intermetallic growth, bend ductility, internal stress, and manufacturing process stability, the GXT plating system clearly outperformed all other gold alternatives including other palladium-nickel and pure palladium coatings.

In fact, in no test did any gold substitute—or gold itself—outperform GXT.

GXT plating, an exclusive Du Pont development, is now available on Du Pont's 0.025″ square pins, including BergStik™ headers, BergPost™ and BergPin™ terminals, and compliant press-fit pins. Some industry leaders already have switched from gold to GXT to help improve the reliability of their products.

If you require high reliability connectors, you're sure to want complete test results. They're yours for the asking...along with sample pins for your own tests/inspection.

Get all the facts! Order this free GXT Convincer Kit.

Review results from independent test laboratories. Proof positive that GXT palladium-nickel plating outwears, outperforms gold. To request kit...

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CIRCLE NO 39

PRODUCTS FOR
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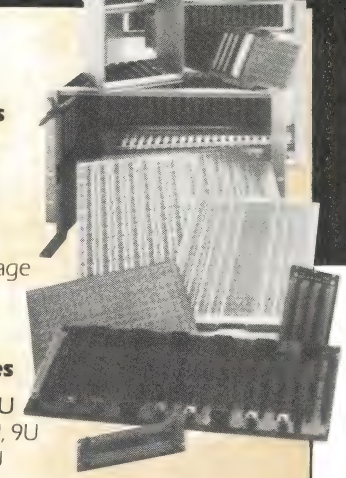
Hybricon, with more experience than any other company in designing, developing and building VME packaging hardware, offers the industry's widest range of both custom and standard VMEbus-configured products . . . all in full production and field-proven.

This VME system has clearly benefited from Hybricon's considerable experience in packaging and interconnection. Components were designed from scratch . . . not adapted from other bus products . . . to best serve VME's unique requirements. Interface flexibility and customer convenience are outstanding, and construction is much more rugged than competitive offerings. It's no wonder that Hybricon VMEbus packaging and interconnection hardware is used on more systems than anyone else's.

In volume production, the best cost/value relationship can often be achieved with a custom design . . . and a significant share of Hybricon's VME business is in custom products. When doing a custom design, Hybricon can draw on an automated database covering over ninety standard VME models . . . speeding the process, saving cost, and greatly reducing the amount of debugging needed.

"EXTRA VALUE DESIGN"

Hybricon's "Extra Value Design" program ensures that industry performance and construction norms are exceeded . . . and that extra features and flexibility will make life easier for the equipment designer. The benefits are evident throughout this VMEbus product system . . . multilayer backplanes with full ground and power planes – factory assembled backplane/card cage combinations in rack, case, drawer and custom mountings – high frequency wire wrappable socket boards with patented VHF design – extensive connector and terminal options – and much, much more.



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J1 in 19" rack mountable cage
6, 9, 10, 11, 12, 15, 16, 20, 21 slots

J1 in optional mount cage
4, 5, 6, 9, 10 slots

Nine 19" Rack Mountable Card Cages

* 21-slot 400mm x 6U, 9U
21-slot 160mm x 3U, 6U, 9U
21-slot 220mm x 6U, 9U
21-slot 280mm x 9U
10-slot 160mm x 6U

Six 160mm Optional Mount Card Cages

4, 5, 6, 9, 10, 12 slots

Eleven J1 Backplanes

4, 5, 6, 9, 10, 11, 12, 15, 16, 20, 21 slots

Eight J2 32-bit Expansion Backplanes

4, 5, 6, 9, 12, 16, 20, 21 slots

Four J2 VMX Expansion Backplanes

3, 4, 5, 6 slots

Six Test Extender Cards

for: J1, 160mm
J1, 220mm
J2, 160mm
J2, 220mm
J1/J2 contiguous, 160mm
J1/J2 contiguous, 220mm

Three Lateral Interconnect Boards

for: J1 to J1
J2 32-bit to J2 32-bit
J2 VMX to J2 VMX

Thirty-two Wire Wrappable Socket Boards

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four 160mm x 6U
four UHD 160mm x 6U
four PGA 160mm x 6U
four UHD 220mm x 6U
four 220mm x 9U
four 280mm x 6U
four PGA 280mm x 6U

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CIRCLE NO 40

High-level software simplifies use of PC-based instrument modules and systems

Chris Everett, *Regional Editor*

Standard application and control programs *shorten test development times on Hewlett-Packard's Vectra personal computer. The computer uses a proprietary bus to control Hewlett-Packard's PC-based instrument modules.*

Today you can easily figure out how to operate any benchtop instrument without picking up the user's manual. If you have to program an instrument for an ATE application, however, you will probably find yourself buried deep in a very un-English-like language just to get the instrument to take a simple reading. If you could bring the ease of front-panel instrument control to the task of programming instruments for benchtop testing or ATE applications, test-program development times would surely drop. Manufacturers of personal-computer-based instruments recognize the value of shortened development times, and in their systems they have incorporated high-level software that lets you enter simple programming commands through "pseudo" front panels displayed on the personal computer's screen.

Many instruments and instrument systems employ a proprietary language, or several proprietary languages, with their own mnemonics and protocols. The IEEE-488 bus specification does not offer much help in sorting out this programming morass. The specification standardizes the physical passing of signals from one instrument to another, but it does not provide guidance as to what form the signals should assume. Several questions remain: Do you use ASCII or BCD data formats? Is the most-significant digit transmitted first or last? How do you signify the end of a data transmission? What language should you use for the test program? Each instrument manufacturer that intends to build GPIB-compatible systems develops its own answers to these questions. The instruments have their own language, data formats, and protocols, and still they all meet the IEEE-488 specification.

Some manufacturers, such as Tektronix, have published the codes, protocols, and formats used by all their instruments. If you're building a benchtop test system that includes Tektronix instruments and controllers exclusively, your integration and programming task is greatly simplified by the common set of codes, protocols, and formats.

One command transfers settings

When it developed this unified approach to building instrument systems, Tektronix simplified the task of programming one step further. The company's engineers reasoned that it's easier to set up and take a measurement using the front-panel controls of an instrument instead of writing a string of commands at the controller. Consequently, they developed a programming command, "SET?," that would cause an instrument to send all its front-panel control settings, and other related information needed to make a measurement, to the controller. You can incorporate that information directly into a test program.

Under the Tektronix scheme, you essentially write your test program by manually setting the front panel of each instrument and setting the signal source needed for a measurement. You then use the SET? command to relay the command string

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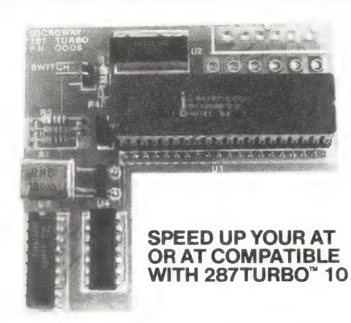

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[1] Requires RTOS or iRMX-86. All Intel compiler names and iRMX-86 TM Intel Corp.

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8087 5 MHz For the IBM PC, XT and compatibles.	**$114**
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287Turbo™ 10 MHz If you own an AT, Deskpro 286 or AT compatible, this is the card you need to get reasonable numeric performance. It plugs into your 80287 socket and includes a specially driven 10 MHz 80287. The card comes in three configurations. The IBM AT version includes a hardware RESET button **$450**

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CIRCLE NO 46

back to the controller and repeat the process for the next measurement step. Several PC-based instrumentation systems now employ this same type of process, but instead of setting the controls on the front panel of a PC-based module, you set the controls on pseudo front panels that appear on the personal computer's screen.

Soft panels, on-card circuitry

In Virtual Instrument's Virtual Cat system, all three of the instrument's pseudo, or soft, front panels are displayed simultaneously on the PC's screen. The measurement hardware is a 2-card module tucked into the PC's chassis. On the cards are measurement and control circuitry for a digital multimeter (DMM), a timer/counter, and a function generator. (**Table 1** lists specifications of all the systems described in this article.)

You manipulate the panels' switches with the cursor keys or with a mouse. Setup changes are implemented immediately; you don't effect the changes by hitting another key, as you do with other instruments. If you do run into an operational problem—an incorrect setup, for example—or if you simply have questions about the setup procedure, you can call up a help menu for instructions.

You can save instrument setups and recall them later. You can also log measurement results along with the date, the time, and comments. The resulting file submits to further processing by Lotus 1-2-3 and other postprocessing programs.

You can also use the Virtual Cat system in an automatic test environment. You write test programs in either Basic or Forth. Although the Virtual Cat system does not have a signal multiplexer, you can use an IEEE-488-controlled multiplexer and other IEEE-488 measurement, stimulus, and recording equipment to complete the system.

Separate chassis has more room

Because of the space limitations within a personal computer's chassis, Vistar's PC1000 system supplies a separate chassis to hold individual instrumentation modules. The expansion chassis (**Fig 1**) has a built-in power supply to drive as many as seven instrument modules. Actually, the PC1000 system software can support two expansion chassis at one time, each with a full complement of seven instruments.

The back of each instrumentation module plugs into the chassis, which is an extension of the IBM PC Bus and connects to the PC via cable. The front of each module is blank except for one or two D-subminiature connectors, to which you can directly wire your signal inputs and outputs for ATE applications. For manual applications, you can insert optional hardware front panels that have the traditional BNC or banana-type plugs. Alternatively, you can plug a signal multiplexer into the D-subminiature connector. The additional pins on the connector pass matrix programming information to the multiplexer.

If you find that Vistar does not supply a desired instrumentation module, such as a scope, you have two options. You can connect the desired instrument via the system's IEEE-488 interface, which includes both the hardware and software needed to tie IEEE-488 instruments into the Vistar operating system, or you can use the 60 in^2 of breadboard space on Vistar's prototype module to build your own instrument. The prototype module includes a parallel interface, a serial interface, an instrument trigger, interrupt lines, and onboard power supplies. It also has a 500-byte EEPROM that you can use to store calibration coefficients, linearization coefficients, or title information that you can call up on the module's front-panel display.

The instrumentation system operates under its own proprietary operating system. If you need to execute a DOS command or run an applications program, you can do so without leaving the Vistar operating system.

The operating system lets you run the system in one of three modes: manual, automatic, and step. In the manual mode, you engage a particular instrument module by calling it up with a key on the personal computer's keyboard or by pressing the Report key on the module's optional front panel. When the instrument's soft front panel appears on the personal computer's

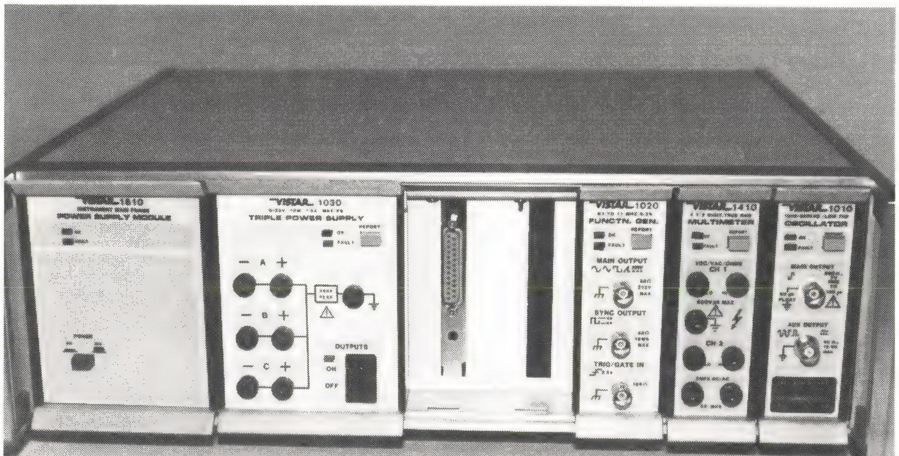

Fig 1—Individual instrument modules plug directly into the IBM PC Bus *when they are inserted into Vistar's expansion chassis. You control DMM, function-generator, power-supply, and timer/counter modules manually from the PC's screen or automatically from a test program written on the PC.*

Text continued on pg 66

TABLE 1—PC-BASED ANALOG INSTRUMENTATION

PRODUCT SERIES	HEWLETT-PACKARD	SUMMATION	VIRTUAL INSTRUMENT	VISTAR
	PC INSTRUMENT SYSTEM	SIGMASERIES	VIRTUAL CAT	PC1000
OSCILLOSCOPE	$1500	$4950	NONE	NONE
NUMBER OF CHANNELS	2	1		
EQUIVALENT BANDWIDTH	50 MHz	N/A		
MAX DIGITIZING RATE	5814 SAMPLES/SEC	10M SAMPLES/SEC		
VERTICAL RESOLUTION	8 BITS	8 BITS		
MIN VERTICAL RANGE	40 mV	50 mV		
DMM	$650	$995	INCLUDED	$875
NUMBER OF DIGITS	4½	4½	4½	4½
RANGES				
DC VOLTAGE	200 mV TO 200V FS	200 mV TO 500V FS	200 mV TO 200V FS	30 mV TO 300V FS
AC VOLTAGE	200 mV TO 200V FS	200 mV TO 300V FS	200 mV TO 200V FS	300 mV TO 300V FS
RESISTANCE	200Ω TO 20 MΩ FS	200Ω TO 20 mΩ FS	200Ω TO 20 MΩ FS	300Ω TO 30 MΩ FS
ACCURACY (10V DC RANGE)	±0.05% RDG ±4 COUNTS	±0.04% RDG ±2 COUNTS	±0.1% RDG ±1 COUNT	±0.05% RDG ±0.012% FS
MAX READ RATE	12.5 RDG PER SEC	25 RDG PER SEC	25 RDG PER SEC	10 RDG PER SEC
OTHER FUNCTIONS	NONE	AC+DC V	AC A, DC A, dBm	P-P AC V, DC A, AC A, P-P AC A, dBV, AND HV Ω (DIODE TEST)
TIMER/COUNTER	$900	$1850	INCLUDED	$1250
FREQUENCY RANGE				
CHANNEL A	10 Hz TO 100 MHz	100 μHz TO 200 MHz	10 Hz TO 100 MHz	0.1 Hz to 120 MHz (1-GHz OPTION)
CHANNEL B	10 Hz TO 2.5 MHz	100 μHz TO 200 MHz	10 Hz TO 2.5 MHz	0.1 Hz TO 3 MHz
TIME INTERVAL RESOLUTION				
SINGLE EVENT	100 nSEC	100 nSEC	100 nSEC	100 nSEC
REPETITIVE EVENT	N/A	±LSD $\pm\frac{1}{\sqrt{\text{NO OF EVENTS AVG}}}$	N/A	3 nSEC
OTHER FUNCTIONS	PERIOD, TOTALIZE, RECIPROCAL FREQUENCY, PERIOD MEASUREMENT	PERIOD, RATIO, TOTALIZE	PERIOD, PULSE WIDTH AVG RATIO, TOTALIZE	PERIOD, RATIO, PHASE, TOTALIZE
FUNCTION GENERATOR	$1500	$2650	INCLUDED	$1250
FREQUENCY RANGE	0.5 Hz TO 5 MHz	0.01 Hz TO 10 MHz	0.01 Hz TO 10 MHz	0.01 Hz TO 11 MHz
WAVEFORMS	SINE, SQUARE, TRIANGLE, RAMPS, PULSES	SINE, SQUARE, TRIANGLE, RAMPS, PULSES	SINE, SQUARE, TRIANGLE	SINE, COSINE, TRIANGLE, SQUARE, RAMP
MODES	CONTINUOUS, BURST, GATED	CONTINUOUS, BURST, GATED	CONTINUOUS, BURST, GATED	CONTINUOUS, TRIGGERED, GATED
AMPLITUDE RANGE	8 mV TO 10V P-P	5 mV TO 10V P-P	5 mV TO 10V P-P	1.5 mV PEAK TO 15.0V PEAK
POWER SUPPLY	NONE	NONE	NONE	$1250
NUMBER OF OUTPUTS				3
POWER RATING				30 (10W PER OUTPUT)
VOLTAGE RANGE				0 TO 24V
VOLTAGE ACCURACY				0.5%
MULTIPLEXER			NONE	$450
NUMBER OF CHANNELS				
ANALOG SIGNAL	8 (HP61011AA, $650)	60 (HDS10, $995)		16
DIGITAL INPUT	16 (HP61010AA, $650)	32 (DIL10, $995)		8
DIGITAL OUTPUT	16	32 (DOL10, $995)		16
RELAY ACTUATOR	8 (HP61017AA, $650)	32 (DPO10, $995)		NONE
OTHER MODULES	DUAL VOLTAGE DAC ($800), DATA ACQUISITION SOFTWARE ($400)	CUSTOM FUNCTION MODULE ($595), HIGH-ACCURACY SWITCHING MODULE ($995), HIGH-FREQUENCY SWITCHING MODULE ($995)	NONE	OSCILLATOR ($950), PROTOTYPE INSTRUMENT MODULE ($350)
GPIB INTERFACE	$400	INCLUDED 300k-BYTE/SEC DMA TRANSFER	$395	$360 200k-BYTE/SEC DMA TRANSFER
CONTROLLER REQUIREMENTS	PC/XT/AT OR COMPATIBLE, HP 150 TOUCH-SCREEN PC/MAX PC/11, HP VECTRA; 640k-BYTE RAM	PC/AT OR COMPATIBLE; 640k-BYTE RAM	PC/XT/AT OR COMPATIBLE; 512k-BYTE RAM	PC/XT/AT OR COMPATIBLE
CONTROL BUS	HEWLETT-PACKARD PROPRIETARY BUS	IEEE-488	PC BUS	PC BUS
ARCHITECTURE	EACH INSTRUMENT MODULE HAS INDIVIDUAL POWER SUPPLY, WHICH CAN BE STORED IN OPTIONAL SYSTEM POWER UNIT. SYSTEM SOFTWARE SUPPORTS EIGHT INSTRUMENTS PER INTERFACE.	EXPANSION CHASSIS WITH POWER SUPPLY SUPPORTS 12 INSTRUMENT MODULES. MODULES ARE CONNECTED WITH VME BUS, HIGH-VOLTAGE BUS, HIGH-FREQUENCY BUS, AND CROSS-TRIGGER BUS.	MODULE INTERNAL TO PC (TWO SLOTS) CONTAINS ALL THE MEASUREMENT AND CONTROL CIRCUITRY.	EXPANSION CHASSIS WITH POWER SUPPLY SUPPORTS SEVEN INSTRUMENT MODULES. SYSTEM SOFTWARE SUPPORTS 14 INSTRUMENTS.
PRICE (CHASSIS AND INTERFACE)	$500	$9950	$1995 INCLUDES OPERATING SYSTEM PLUS DMM, FUNCTION GENERATOR, AND TIMER/COUNTER MEASUREMENT CAPABILITIES	$1770

KEY:
N/A = INFORMATION NOT AVAILABLE RDG = READING

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screen, you can change setup parameters and read the results immediately. You can even change the setup of another module by typing in a command string. For example, while you're viewing the frequency counter's front panel you can type "SET FGEN1, FRQ=200KHZ" to change the output frequency of the function generator.

You write fully automatic test programs by incorporating these same command strings in Basic code. Vistar provides the header routine; the string variable "CMD$" lets the system know that code following it is a command.

A second way to develop an automatic test program is to use the system's snapshot feature. You set all your instrumentation controls for a particular measurement, and then you take a "snapshot" of (that is, save) the entire setup for incorporation into the test program. Step-mode operation takes advantage of this capability, recalling such snapshots when needed to take simple, repetitive measurements.

If you're using the Vistar system in a production test environment, you may want to use the Vinstall software package to develop your test programs. Vinstall lets you write and debug a test program using simulated instruments instead of the actual hardware. The software runs on the IBM PC, PC/XT, or PC/AT, so you can, for example, develop your program on the IBM PC and transfer it to a PC/AT on the manufacturing floor to achieve faster test execution times.

Like Vistar, Hewlett-Packard has chosen not to design its PC Instrument System modules as residents of the personal computer itself. Unlike Vistar, however, Hewlett-Packard packages each measurement module in its own case, each case having its own power supply. As a consequence, the potential for crosstalk and other noise problems is significantly lower. This is one of the reasons why Hewlett-Packard can offer a scope module with a 50-MHz effective bandwidth.

Instead of using the IBM PC bus or one of the other existing, standard buses to connect the modules to the controller, Hewlett-Packard has developed a new bus, the PCIB. The PCIB is a hybrid bus consisting of two independent communication channels: an 8-bit parallel bus and a serial bus. Those modules that need to send large quantities of data back to the controller, but don't need to be electrically isolated to take measurements, employ the 8-bit parallel bus. (The scope module is one example.) The DMM module and other modules that must maintain electrical isolation from each other and from the controller use the serial channel. Because both channels use the same communication protocols, however, you can't tell which channel is in use.

You can use the PC Instrument System with either the IBM family of PCs or with Hewlett-Packard's Vectra and HP 150 Touchscreen computers. If you're using an IBM PC, you can also use the IBM mouse to change setups on the measurement modules' soft front panels. If you're using the Touchscreen computer, you can change settings on the soft front panel with your finger.

The personal computer displays a status window next to each module's soft front panel. The status window gives a continuous reading of the measurements that the module is taking, or of the outputs provided by all the other modules in the system.

You cannot change an instrument parameter through the status window, however. For example, if you want your main display to be the scope front panel so you can view the pulse parameter measurements as well as the trace, you can't use a line command or a menu command to change a parameter on the function generator. You must first save the scope panel, then call up the function-generator panel to make your setup change. Then you save the function-generator panel and return to the scope panel to view the results.

You write automatic test programs in Basic. Two generic commands, Output and Measure, let you program many of the modules without having to learn many different commands for each module. Also, you can manually set up your instruments and store the settings in a file that a test program can call.

After the system collects data, you can use HP's $400 data-acquisition software package to list or plot your results. The data-acquisition package also has application pro-

Debugging aids, *such as code tracing, a trace stack, IEEE-488 statement tracing, and breakpoint controls, speed the development of test programs for the Summation Sigmaseries tester, an integrated analog/digital test system.*

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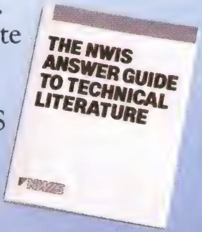


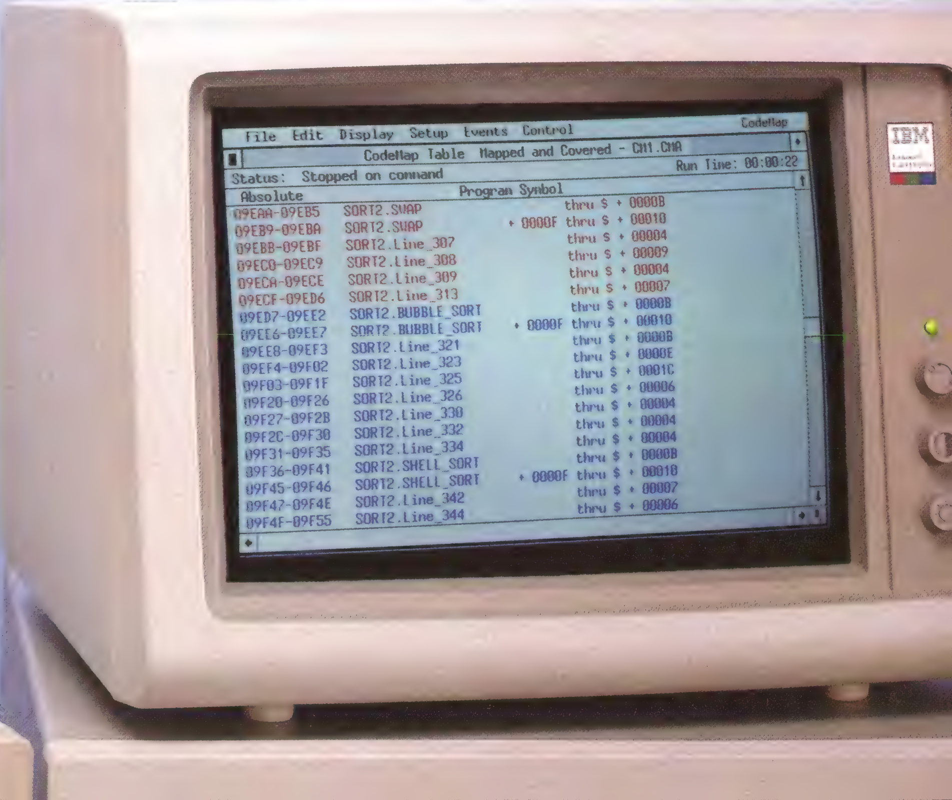
Circle No 45 For Demonstration

Circle No 6 For Literature

NWIS

NORTHWEST INSTRUMENT SYSTEMS, INC.

Am Eichenhag 12
8160 Miesbach, West Germany
Phone: (49) 8025-3260; Telex: 526938



```
CodeMap Table  Mapped and Covered - CM1.CMA
                                              Run Time: 00:00:22
Status:  Stopped on command
 Absolute                  Program Symbol
09EAA-09EB5   SORT2.SWAP                    thru $ + 0000B
09EB9-09EBA   SORT2.SWAP           + 0000F thru $ + 00010
09EBB-09EBF   SORT2.Line_307                thru $ + 00004
09EC0-09EC9   SORT2.Line_308                thru $ + 00009
09ECA-09ECE   SORT2.Line_309                thru $ + 00004
09ECF-09ED6   SORT2.Line_313                thru $ + 00007
09ED7-09EE2   SORT2.BUBBLE_SORT             thru $ + 0000B
09EE6-09EE7   SORT2.BUBBLE_SORT    + 0000F thru $ + 00010
09EE8-09EF3   SORT2.Line_321                thru $ + 0000B
09EF4-09F02   SORT2.Line_323                thru $ + 0000E
09F03-09F1F   SORT2.Line_325                thru $ + 0001C
09F20-09F26   SORT2.Line_326                thru $ + 00006
09F27-09F2B   SORT2.Line_330                thru $ + 00004
09F2C-09F30   SORT2.Line_332                thru $ + 00004
09F31-09F35   SORT2.Line_334                thru $ + 00004
09F36-09F41   SORT2.SHELL_SORT              thru $ + 0000B
09F45-09F46   SORT2.SHELL_SORT     + 0000F thru $ + 00010
09F47-09F4E   SORT2.Line_342                thru $ + 00007
09F4F-09F55   SORT2.Line_344                thru $ + 00006
```

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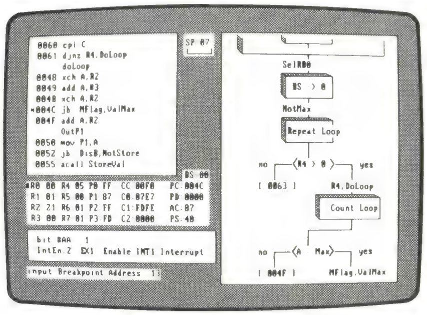

```
0060 cpl C
0061 djnz R4,DoLoop
     doLoop
0048 xch A,R2
0049 add A,R3
004B xch A,R2
*004C jb  MFlag,ValMax
004F add A,R2
     OutP1
0050 mov P1,A
0052 jb  DisB,NotStore
0055 acall StoreVal
```

```
SP 07
BS 00
*R0 00 R4 05 P0 FF  CC 00F0  PC 004C
 R1 01 R5 00 P1 07  C0 07E7  PD 0000
 R2 21 R6 01 P2 FF  C1:FDFE  AC:07
 R3 00 R7 01 P3 FD  C2 0000  PS:40
```

```
bit #AA   1
IntEn.2  EX1  Enable INT1 Interrupt
input Breakpoint Address  13
```

(8051 debug/simulator shown)

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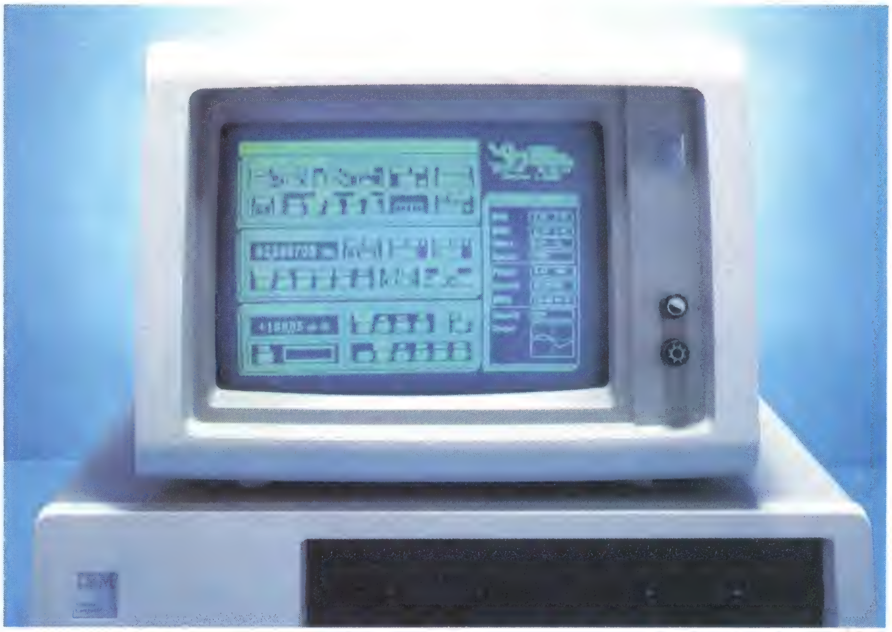

In PC-based instrumentation systems, you change measurement setups *by manipulating pseudo, or soft, front panels displayed on the PC's screen. This instrumentation system, Virtual Instrument's Virtual Cat System, consists of a 2-card module located in an IBM PC.*

grams that run your measurement system as a voltage scanner, thermocouple scanner, or analog recorder. Standard utilities in the package reformat your data for use by Lotus 1-2-3, Visicalc, Wordstar, or any other application program requiring stripped ASCII or Data Interchange Format (DIF) formatted data.

Another alternative is to control your PC Instrument System using Macmillan Software's (New York, NY) Asyst software package. Asyst's statistical and graphics subroutines help process your data.

Up to a point, Summation Inc's approach to the design of PC-based instrument systems is the same as Vistar's and Hewlett-Packard's: Measurement modules should be housed outside of the personal computer. However, to achieve tighter coordination—that is, direct communication—between modules, Summation's Sigmaseries test system uses a single, "active" chassis with two additional buses. The Sigmaseries chassis holds as many as 12 modules. You can add a second chassis to the first if you need additional capabilities.

The system's chassis is active in the sense that it's controlled by a 68000 μP. In fact, the chassis can run test programs independently of the personal computer's control. The chassis can interact with an operator through the chassis's seven special-function keys and 2-line×40-character alphanumeric display.

The 68000 controls the modules over the VME Bus, which can pass data at a 300k-byte/sec rate. In addition, the measurement, stimulus, and switching modules are all tied together by an analog data bus. Two of the bus lines can handle 1-MHz signals to 500V at 2A, while the other 10 data lines are for low-voltage, high-frequency signals. A third bus, the cross-trigger bus, connects all the measurement modules to the stimulus modules. The system can trigger measurements with less than 50-μsec delays.

The chassis connects to the PC/AT via the IEEE-488 bus. As a result, it's very easy to incorporate stand-alone IEEE-488 instruments into the system.

Although you can use the Sigmaseries tester in a manual test mode, it's primarily intended for use in an

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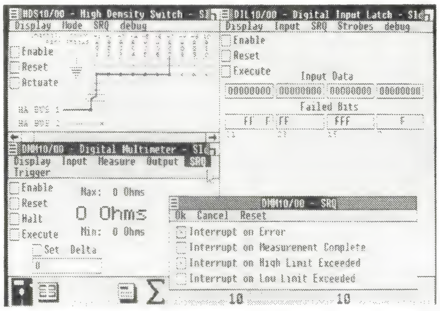
ATE environment. You program the modules through a series of icons and interactive pull-down menus. Each module window has a display area that presents measurement results or permanently active controls, such as the frequency/amplitude scroll bar in the function-generator window. To change settings, you use the mouse to pull down the setting menu and make your changes via the keyboard. You can also pull down a status menu, which shows the current system or device status, including all error messages.

The switching-matrix modules have display areas that show the signal routing through the matrix and onto the analog bus. You can program the matrix by connecting dots on the switching map.

You can write test programs interactively, using the device windows to make instrument setups and the Basic editor window to write code. When you are satisfied with a test setup, you transfer it to the Basic editor window, where the setups are converted to the appropriate IEEE-488 commands.

Several features help you troubleshoot your program. The trace-code tool traces the path of program execution for each routine. The trace stack keeps track of the active subroutine calls. The trace variable lets you list the values of a specific variable during program execution. You can trace the flow of IEEE-488 statements to and from the IEEE-488 bus. All of these debugging tools can operate simultaneously.


HDS10/00 - High Density Switch - S1
Display Mode SRQ debug
Enable
Reset
Actuate
DIL10/00 - Digital Input Latch - S1
Display Input SRQ Strobes debug
Enable
Reset
Execute
Input Data
00000000
00000000
00000000
00000000
Failed Bits
FF F
FF
FFF
F
DMM10/00 - Digital Multimeter - S1
Display Input Measure Output SRQ
Trigger
Enable
Reset
Halt
Execute
Max: 0 Ohms
0 Ohms
Min: 0 Ohms
Set Delta
0
DMM10/00 - SRQ
Ok Cancel Reset
Interrupt on Error
Interrupt on Measurement Complete
Interrupt on High Limit Exceeded
Interrupt on Low Limit Exceeded
10
10

Icons and pull-down menus with soft-front-panel displays *help you write test programs on an IBM PC/AT for Summation's Sigmaseries tester.*

Summation estimates that its graphical programming techniques reduce test-program generation times by as much as 80%. Hewlett-Packard and Vistar representatives agree that shorter program-development times are a major competitive advantage of PC-based instrumentation systems over other types of instrumentation systems. Yet this advantage is currently offset by limited capability; 4½-digit multimeters and 50-MHz scopes don't meet the measurement needs of many design engineers. Improved capabilities—and lower prices—are the keys to widespread acceptance of PC-based instrumentation. **EDN**

Article Interest Quotient
(Circle One)
High 500 Medium 501 Low 502

For more information . . .

For more information on the PC-based instrumentation systems described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Hewlett-Packard Co
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Palo Alto, CA 94303
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Circle No 646

Virtual Instrument Corp
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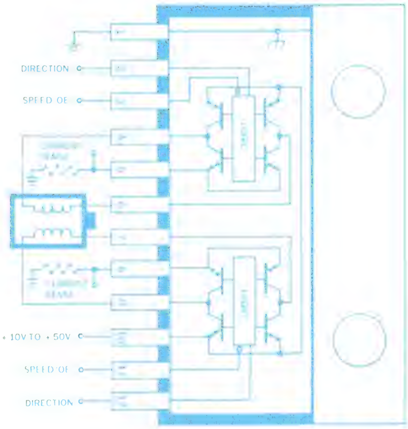

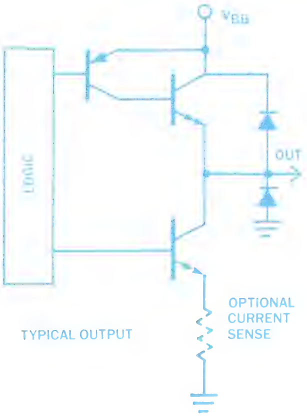

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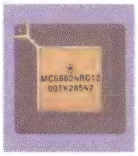

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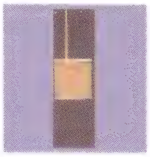

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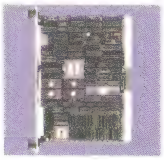

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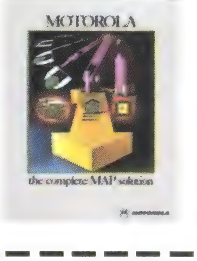

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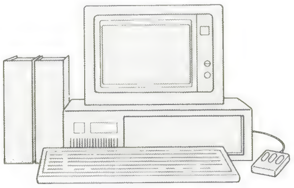

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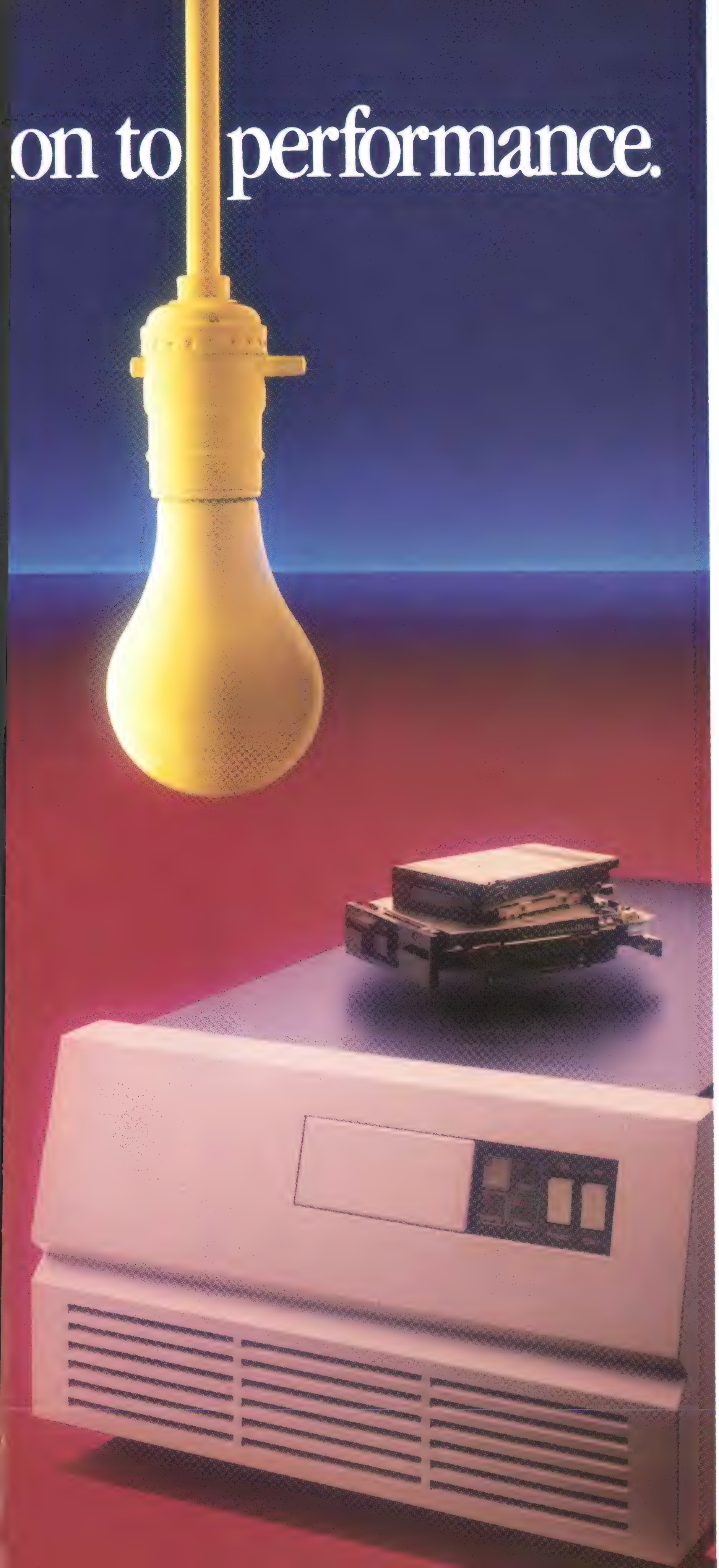

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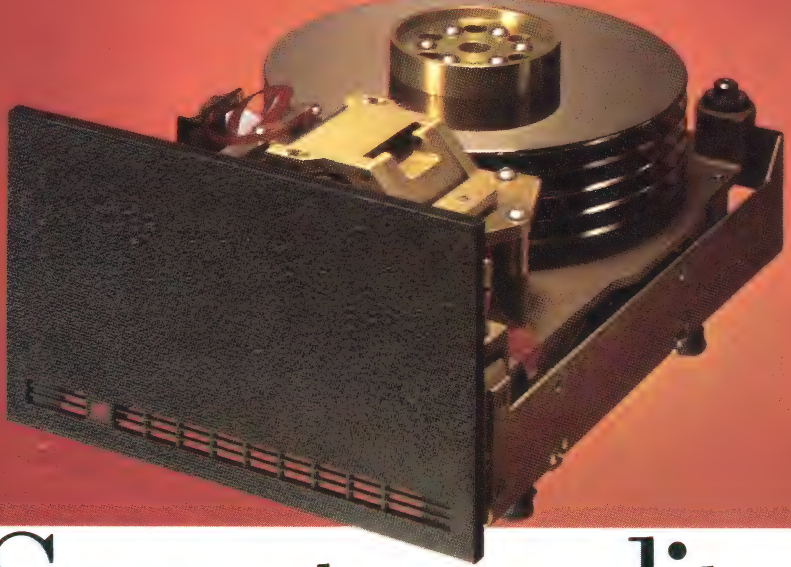

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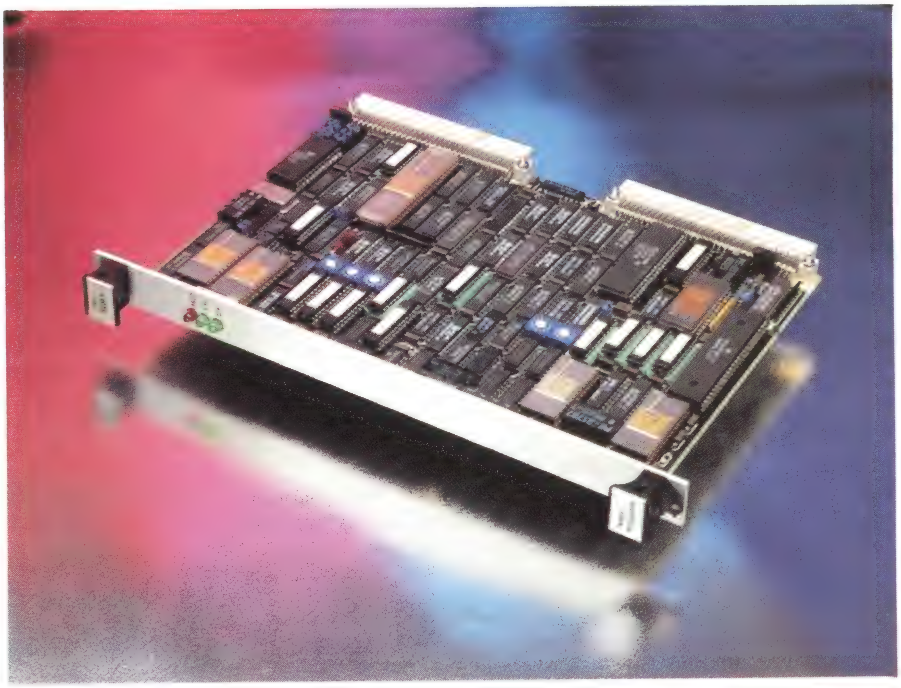
SCSI host-adapter boards meet the needs of Multibus and VME Bus computer systems

Maury Wright, *Regional Editor*

You buy, rather than design, boards to hurry a product to market, and now you can obtain Small Computer System Interface (SCSI) capabilities in board form for your system designs. SCSI host adapters, with varying complexities and capabilities, suit a wide variety of VME Bus and Multibus I system needs, and they'll soon serve Multibus II needs as well. Remember, however, that the SCSI spec is just one approach among many to system configuration, and take care to ensure that the SCSI in general, and your chosen host adapter in particular, is the best match for your application.



Sixteen concurrent operations *execute under firmware control in a system that incorporates the SCSI-1 host adapter from Plessey Microsystems.*

The SCSI standard offers the system designer many advantages over other types of host-peripheral connection—most notably flexibility and performance. You can connect a variety of peripherals to a system through a single interface. The interface handles data transfers at a maximum 1.5M-byte/sec asynchronous rate and at a maximum 4M-byte/sec synchronous rate. Furthermore, the standard allows multitasking capabilities within the I/O subsystem; when I/O devices receive a command, they can disconnect themselves from the SCSI bus while they perform the operation. The bus is therefore free to handle other I/O operations while peripherals perform lengthy tasks.

Standard board reduces cost

In its simplest form, the SCSI bus connects peripherals to a computer. Because SCSI circuitry fits between the system bus and the device-level interface, it's an intermediate I/O bus, as opposed to the device-level interfaces now found on most peripherals. Consequently, use of the SCSI I/O bus may increase cost; in single-host, single-peripheral systems, for example, host-resident, device-level controllers provide a direct, efficient connection. When the number of peripherals (and hosts) begins to climb, however, the SCSI bus proves economical because it connects all peripherals through one interface.

You should keep a couple of other factors in mind when considering SCSI host adapters—particularly at the high end. The SCSI committee is working on a subset of the standard, called the Common Command Set (CCS), which is a subset of SCSI commands. The need for the CCS exists because SCSI products that employ different options defined by the standard can be incompatible with one another. Inclusion of the CCS in future SCSI products should render them all compatible with one another.

Peripheral-controller boards implement the CCS on board. Host-adapter data sheets often list the CCS as a feature, but you must remember to incorporate the CCS operations in your SCSI I/O-driver routines.

You should also note that some companies use the terms SCSI and SASI (Shugart Associates System Interface) interchangeably. The SCSI standard originated from SASI, which is now a subset of the SCSI spec. Make sure the vendor you're dealing with offers the full SCSI spec and not the SASI subset.

SCSI configurations vary from single-host, single-peripheral systems to those with multiple hosts and multiple peripherals. Special needs arising from such variety may dictate that you design your SCSI

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μPD43256-15	32K x 8	150	150	11	385
μPD43256-10L	32K x 8	100	100	.55	385
μPD43256-12L	32K x 8	120	120	.55	385
μPD43256-15L	32K x 8	150	150	.55	385

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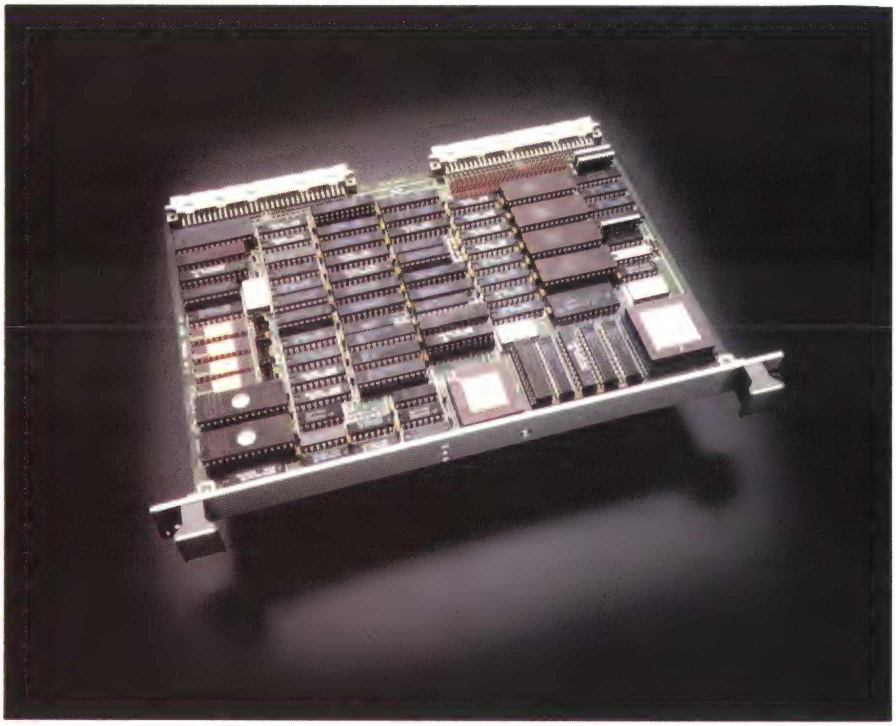


***Synchronous data-transfer rates of 4M bytes/sec,** the specified SCSI limit, are within the range of Introl's Model 300 VME SCSI host adapter.*

host adapter yourself, to optimize performance. Off-the-shelf host-adapter boards, however, will reduce development cost and time, and they, too, show considerable variety—in capability, ease of use (that is, the amount of firmware included), and cost.

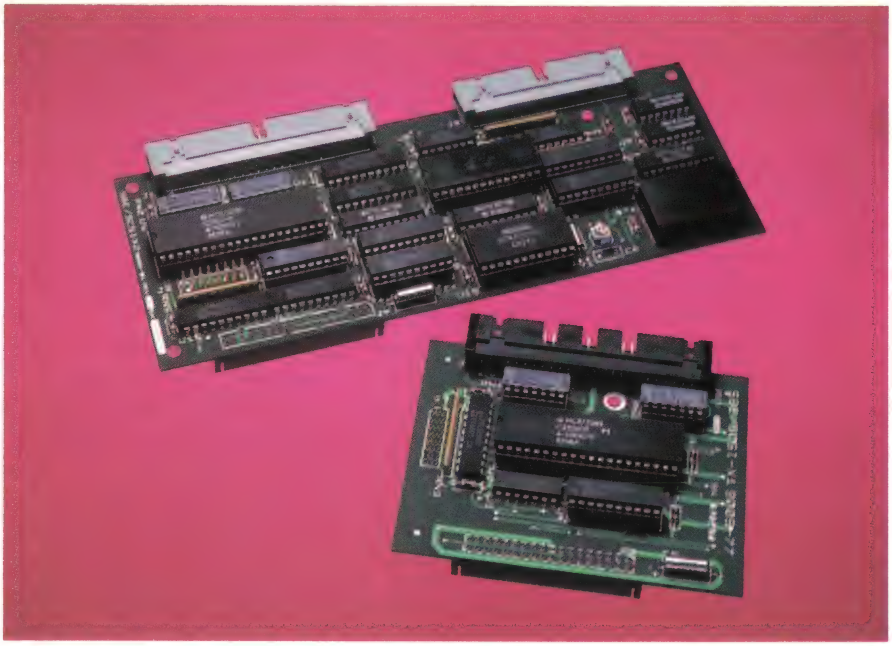
Adapters use SCSI ICs

Specialized ICs (**Ref 1**) for SCSI host adapters also help reduce the cost of using the interface. Simple SCSI host adapters based on such chips can cost less than $500. The Model SCSI and Model SCSI-CP modules from SBE are notable examples. These modules, intended for low- to medium-performance applications (that is, a single host and just a few peripherals operating at speeds no greater than about 800k bytes/sec) include the NCR 5380 SCSI chip. The 5380 consists of SCSI-compatible driver/receiver pairs; the host-CPU board's µP executes the firmware that handles SCSI data transfers. The 5380 will work, however, with a DMA controller for data transfers to Multibus I memory with no µP intervention.

Both the SBE modules allow you to add the SCSI protocol to Multibus I CPU boards in a kind of daughter-board arrangement, connected via an iSBX (Multibus I I/O expansion bus) connector. Data transfers are eight bits wide; when working with a typical SBE CPU board, the modules transfer data at a rate of approximately 500k bytes/sec. Model SCSI costs $165. Model SCSI-CP adds clock/calendar circuitry and a parallel port and costs $320 (100).

The cost of these inexpensive modules, of course, does not reflect the entire cost of using the SCSI. For example, the peripheral must have the SCSI in addition to the device-level interface. Fortunately, specialized SCSI ICs have also made the peripheral SCSI cost reasonable. Emerging peripherals also feature embedded SCSI interfaces, thus eliminating the device-level interface.

In addition to the cost of the SCSI hardware, you must also consider the overall system cost of using the SCSI. When you design a system, you must make the components work together, and that's when software development becomes important. You must, for example, develop software that interfaces the SCSI host adapter to the system's operating system. Operating systems sometimes come with these I/O-driver routines for specific con-



***To adapt a Multibus I system to the SCSI I/O bus,** you can use the Model SCSI-CP (top) or Model SCSI (bottom) iSBX modules from SBE Inc. The SCSI-CP offers clock/calendar circuitry and a parallel port.*

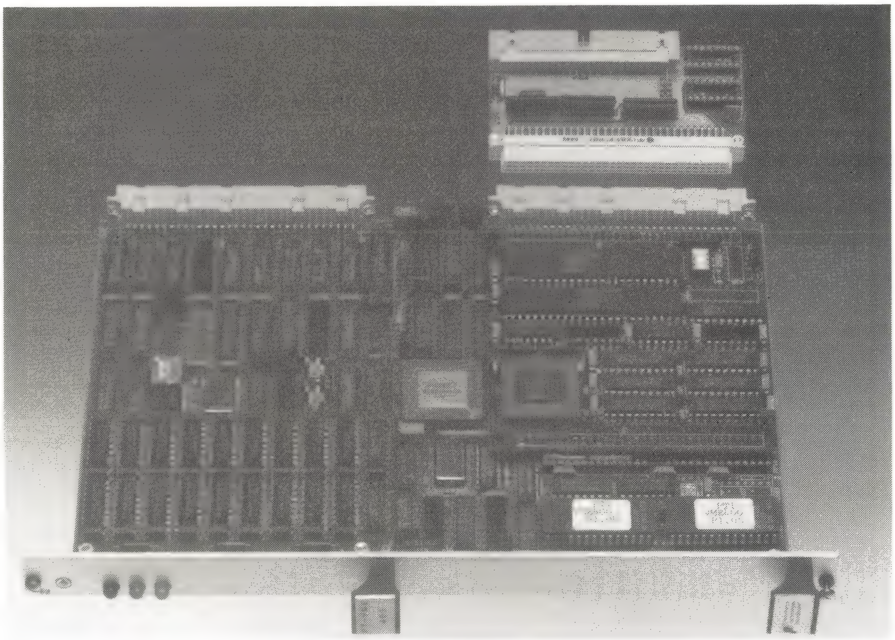
troller boards, but a SCSI I/O driver might not be among them.

There are two schools of thought on the subject of I/O-driver software for operating systems: Use plug- and software-compatible peripheral-controller hardware, or develop your own I/O drivers. As a system designer, you could choose a non-SCSI board for disk or tape I/O from Intel or another manufacturer. Choosing a standard I/O board that's compatible with the host computer's operating system is the safest and quickest way to build a system that works. However, by developing your own SCSI I/O-driver routines for a SCSI-type host adapter, you may achieve higher—and in the long run less expensive—system performance.

Manufacturers of host adapters typically supply sample I/O-driver software for one or more operating systems ("sample" in the sense that you get a basic driver that you must modify or add code to). SBE, for example, provides a sample I/O driver for the Unix-like real-time operating system Regulas. For a higher level of performance, Zendex offers the Multibus I iSBX SCSI modules and I/O drivers for RMX-86, CP/M-86, and Concurrent DOS. These operating systems suit applications that might employ an iSBX SCSI host adapter.

Zendex's ZBX 280 and ZBX 288 SCSI iSBX modules cost $219 and $295 (100), respectively. The latter includes clock/calendar circuitry. The two Zendex modules feature identical SCSI architecture, and they employ the NCR 5380 SCSI IC. Like the SBE modules, the Zendex products depend on a host CPU for control but also work with DMA controllers. According to Zendex, when you use an 80186-based CPU board, your system can achieve data-transfer rates close to the 1.5M-byte/sec SCSI maximum.

Designers of VME Bus-based systems can also economically implement the SCSI spec in low- to medium-performance systems.



A buffer memory with a capacity of 320k bytes *renders the PT-VME400 host adapter from Performance Technologies suitable for high-throughput applications.*

Mizar, for example, offers the Model VME8500 single-height SCSI host adapter for $195 (100). The board appears to the host CPU as two read-only and two write-only registers, on the VME Bus, that the CPU accesses in a programmed-I/O mode. The VME8500 implements the standard without using a SCSI IC; the host adapter employs TTL circuitry and a PLA that works as a state machine to accomplish the SCSI handshake.

Programmed I/O limits speed

Basically, the programmed-I/O mode requires that the host CPU participate in or control all data transfers, unlike the DMA operations available in the SBE and Zendex modules, which transfer data directly to and from memory. Lack of DMA capability limits data rates to the processor's speed, which is typically far less than 1M byte/sec.

Despite the lack of DMA capability, the VME8500 provides a suitable I/O interface for many applications because Mizar offers VME8500 I/O drivers for real-time and general-purpose operating systems. You can choose from I/O drivers for OS-9/68K, PDOS, PolyForth, and CP/M-68K.

All the products mentioned so far target applications that require fairly simple system configurations and data-transfer speeds. The SCSI bus's principal attraction in such applications is its flexibility. For high-performance applications, most of which will be Unix-based systems, other factors will determine whether you'll use the SCSI standard, and which host adapter you'll choose if you do find the spec suitable. Relevant factors influencing the choice of host adapter include the features of the board's SCSI IC, whether the board employs differential or single-ended transceivers, and whether it supports multithreaded operation.

Multithreading for concurrency

Many high-performance applications require a host adapter that operates at the maximum SCSI data-transfer rate. Host adapters that can work at such speeds keep the bus clear and are thus better able to establish several logical threads—that is, communication channels—to various peripherals. Such multithread operations provide multitasking capabilities in the I/O subsystem. A single host, for

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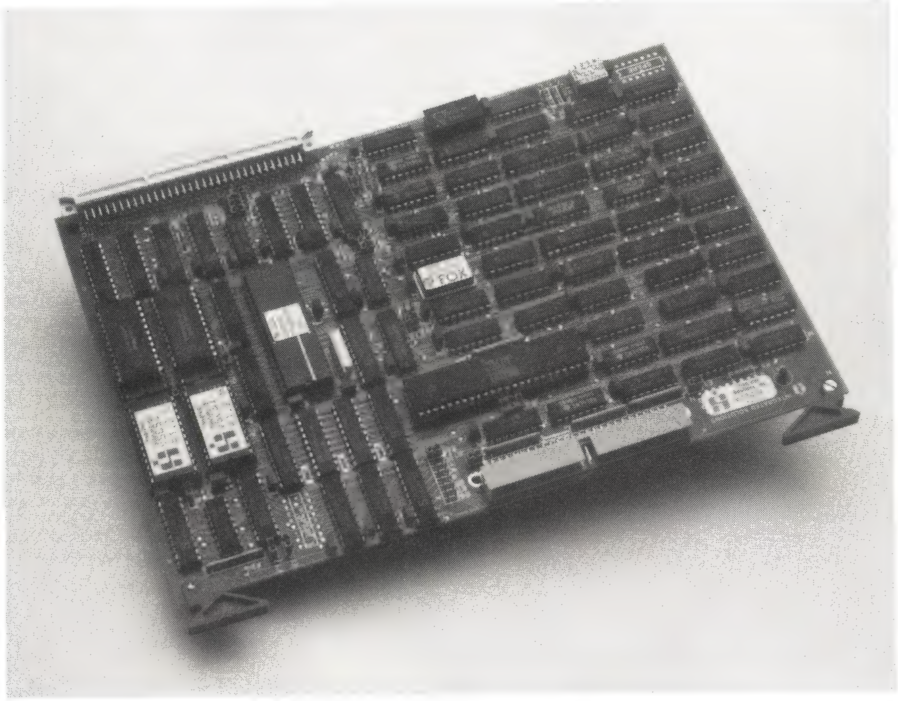
example, may require that different peripherals execute such commands as block reads simultaneously, or multiple hosts in a more complex system may need to communicate with several peripherals and with each other to complete a given task. A SCSI host can support 56 logical threads, but typical systems employ 16 or fewer threads.

High-end host adapters must not only support high data rates and multithread operations; they must do so with as little effect on the host CPU as possible. High-performance host adapters therefore include μPs, DMA controllers, and memory. The ability of the SCSI host adapter to offload tasks from the host CPU also depends on the kind of SCSI IC it incorporates; some SCSI ICs provide such features as DMA capability on chip. Also, manufacturers of high-end host adapters must provide even greater software support than that provided with the simpler adapters. Indeed, operating-system I/O drivers and host-adapter firmware may be the key to your product choice.

NCR was among the first to develop full-featured host adapters. The company uses its ADP-32 Multibus I host adapters in its NCR-tower computers. The $620 ADP-32-03 employs standard single-ended tranceivers that allow total cable lengths of 6m. The $685 ADP-32-04 with differential transceivers extends cable lengths to 20m.

An ADP-32 board includes an 8031 μP, a proprietary DMA controller, and the NCR 5385 SCSI IC. Typical of most high-end host adapters, the board and the controlling firmware employ a mailbox approach to passing commands between the CPU and the host adapter. The CPU writes a command block into the Multibus I main memory and then sends the host adapter a pointer to the command block. The host adapter can handle eight mailboxes, and therefore eight I/O operations, or threads, concurrently (the mailbox approach is a common way to achieve multithread operation).



A Z8000 μP, an NCR 5385 SCSI IC, and a 32k-byte FIFO buffer *are the principal functional components of the VME-GPSCSI host adapter from Integrated Solutions.*

The DMA controller transfers data directly between the SCSI chip and the Multibus. A latch does provide an interface to the bus, but the host adapter provides no memory to serve as a buffer for the data. NCR engineers believe that buffers should be on the device controllers, and that data passes between the system's main memory and the 5385 IC most efficiently via a direct transfer. The DMA controller can perform 8- or 16-bit transfers via the Multibus.

NCR takes an unusual stand on the subject of software support. The company offers an application note that covers the basics of how to write software for the host adapter, but it does not provide a sample Unix I/O driver. The company will consider selling Unix-driver source code to customers who buy in large volumes.

You'll find capabilities similar to those of the NCR ADP-32 in Adaptec's $350 (1000) AHA-1530 Multibus I host adapter. The Adaptec board also employs a mailbox scheme to support eight concurrent operations, and the company has designed custom SCSI circuitry primarily from discrete components. The SCSI circuitry employs a state machine to accomplish the SCSI handshake, and an onboard 8085 μP controls SCSI operations.

Along with the AHA-1530, you get a sample Unix System V I/O driver. Adaptec representatives believe that software support is the key to a host adapter's success. Ed Turner, director of product marketing, states that a system should use custom drivers, rather than plug-compatible peripheral controllers, to achieve the best performance. Turner estimates that developing a driver normally takes three man-weeks to three man-months; when you work from a sample driver, you shorten the development period.

VME boards suit Unix world

Multibus I systems serve some applications in the Unix world, but newer Unix designs are leaning toward the VME Bus and Multibus II. Several companies now offer VME host adapters, and many more VME SCSI products will become

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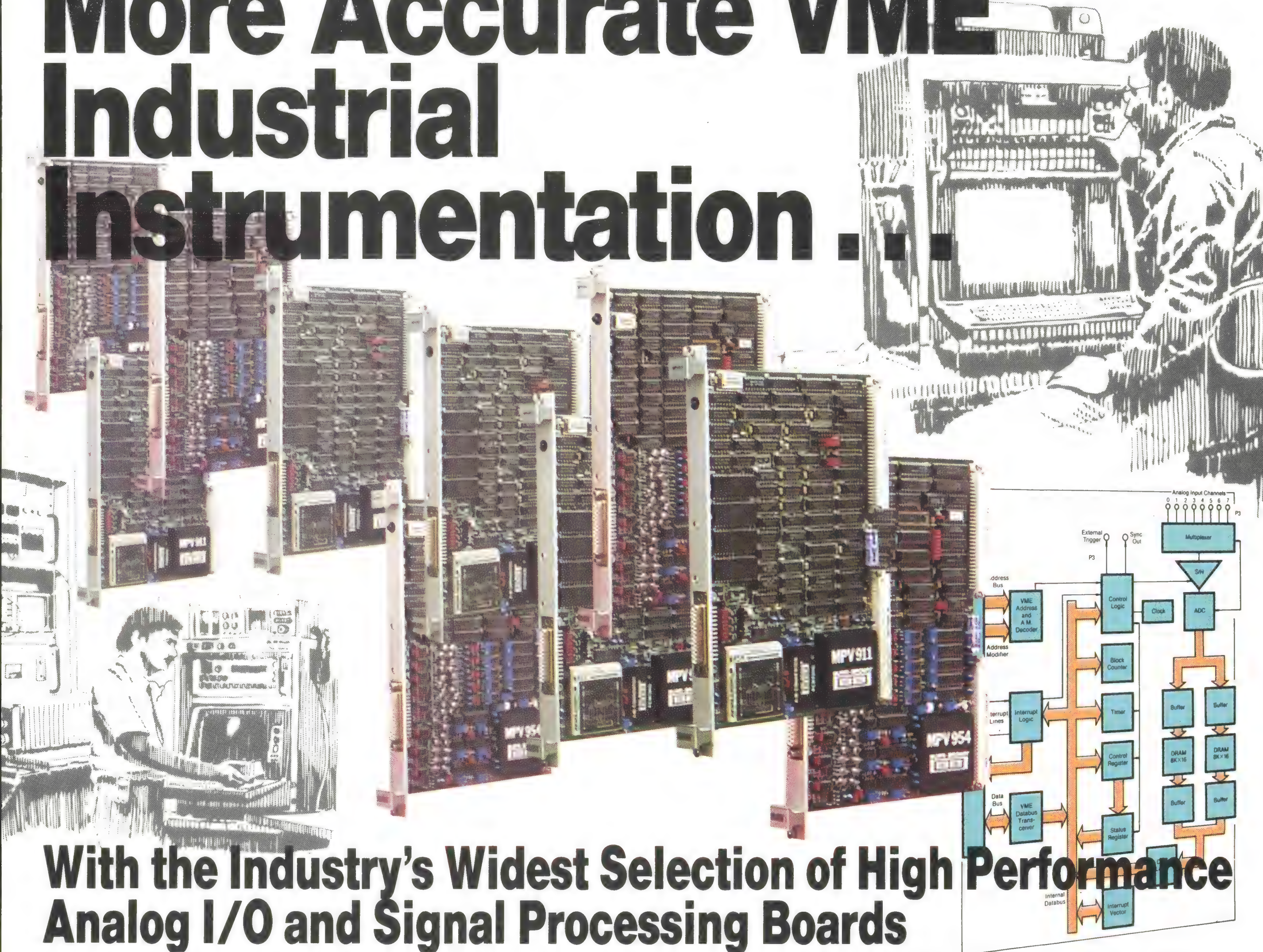

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available within the next year. The VME host adapters offer capabilities similar to those of Multibus I SCSI boards.

Consider, for example, Integrated Solutions' VME-GPSCSI, which costs less than $1000 (100). The company originally designed the board and developed Unix I/O drivers for use with specific Adaptec controllers, but at the hardware level the board is a general-purpose host adapter. Integrated Solutions has developed general-purpose firmware for the board, and it expects to introduce a general-purpose Unix 4.2 driver in the first quarter.

The VME-GPSCSI incorporates an NCR 5385 IC, a Z8000 μP, and 32k bytes of FIFO buffer memory. The Z8000 operates in block mode to perform pseudo-DMA transfers between the 5385 and the FIFO buffer. In addition, the Z8000 transfers data from the FIFO to the VME system's main memory via a 16-bit path. The host CPU passes command blocks directly into registers on the host adapter. This technique precludes multithread operation, but you can make firmware modifications to implement a mailbox-type command-passing approach.

Other VME host adapters do offer multithread operation. The PME SCSI-1 host adapter from Plessey Microsystems supports 16 concurrent operations using a mailbox approach. It operates under the control of a 68008 μP, and it includes a 68430 DMA controller and the NCR 5380 SCSI chip. The DMA controller transfers data between the 5380 and a 2k-byte FIFO buffer. The controller also supports 32-bit DMA transfers over the VME Bus.

Software sets interrupt level

The Plessey host adapter offers programmable interrupt-level selection. Because it receives the interrupt level as a part of the command block, the board supports a multiprocessor environment. When you have multiple CPUs in one system, the SCSI host adapter differentiates between the CPUs according to their respective interrupt levels, which are programmed in the command block. Plessey offers a Unix System V I/O driver for the board, and it plans to offer a Versados driver as well. The PME SCSI-1 costs $1335 (100).

The PME SCSI-1 specs a 1.5M-byte/sec max asynchronous data-transfer rate, as does the SCSI spec. If operation at that speed is essential to your application, be careful when evaluating boards that use the 5380 chip. NCR admits that the chip may have difficulty running at 1.5M bytes/sec, and that 1.25M bytes/sec may be a more reasonable expectation. An imminent CMOS version of the chip will exceed the 1.5M-byte/sec speed. Of course, even 1.25M bytes/sec exceeds the capability of many disk drives.

For those who need more speed—to handle newer breeds of fast disk drives, for example, or to keep channels clear for multithread operation—Performance Technologies offers a host adapter optimized for throughput (it's designed to ensure a 1.5M-byte/sec speed for every transfer). The $1575 (100) PT-VME-400 includes a 68010 μP, an NCR 5385 SCSI IC, a 68450 DMA controller, and 128k bytes of dual-port RAM that can be mapped into the VME address space. The board's 320k-byte buffer memory and the DMA controller ease the transfer of data from a peripheral to the VME system's main memory.

The PT-VME400 manages the SCSI protocol on the vendor-specific pins of the VME Bus's P2 connector. The company also provides hardware to adapt the VME connector to a standard flat-cable connector. The board also comes with a sample Unix driver. The SCSI firmware supports four concurrent threads.

Single-board CPU adds SCSI

Performance Technologies' SCSI host adapters are really adaptations of a general-purpose, 68010-based CPU board. When you buy the full SCSI host adapter, the board comes without certain CPU-board features, such as a real-time clock, a

For more information . . .

For more information on the host-adapter boards discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

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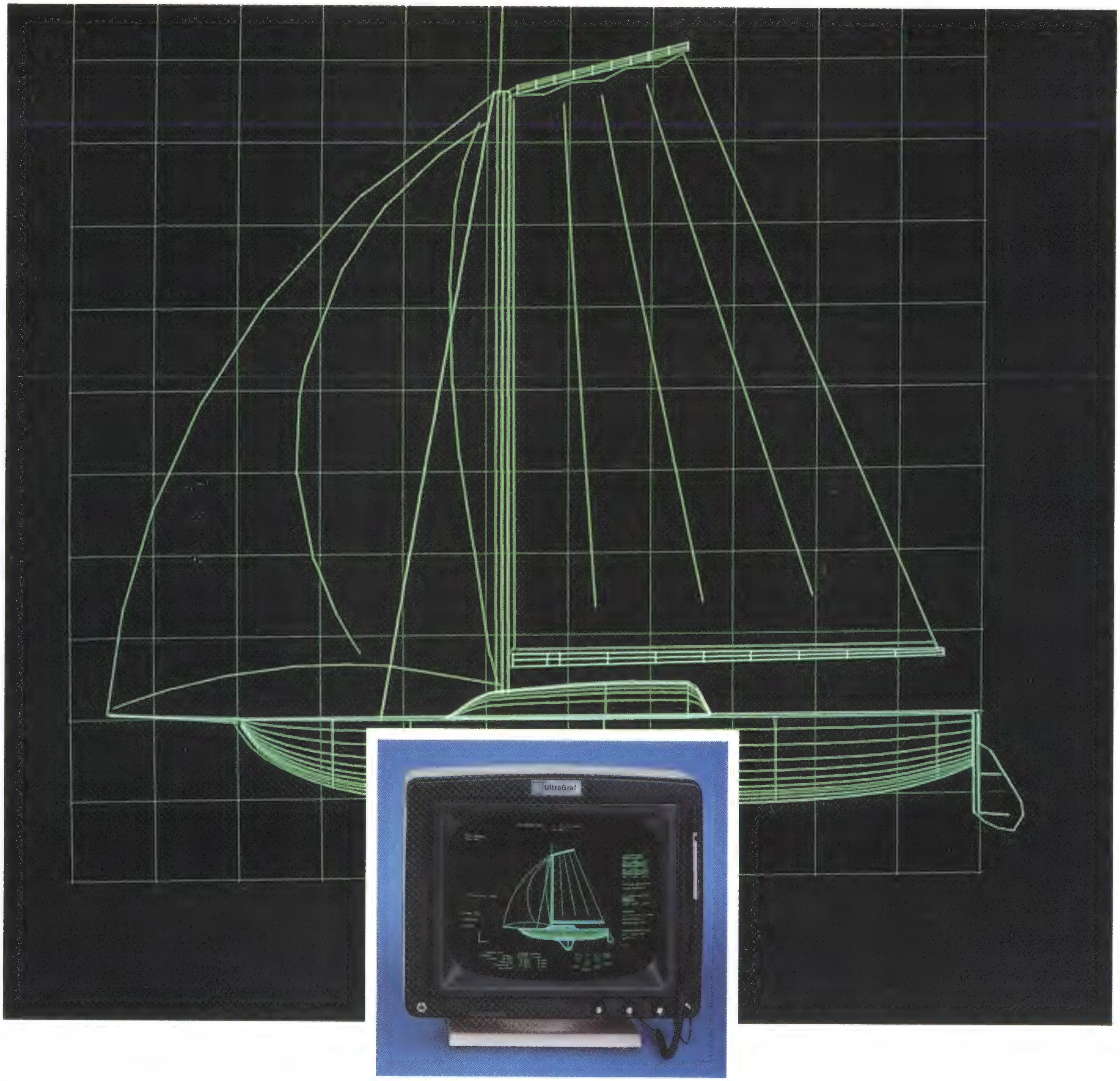

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system controller, and an interrupt handler. The 68010 µP contains the SCSI firmware. The SCSI circuitry resides on a daughter board.

When it's dedicated to SCSI firmware, the 68010 µP obviously has no time to manage other functions. You can, however, buy the CPU board with the PDOS real-time operating system and abbreviated SCSI capability for a simple, low-performance application—for example, in an industrial-control environment. This version, the PT-VME102, comes as a single-board computer with on-board SCSI circuitry and the real-time operating system for $1875 (100).

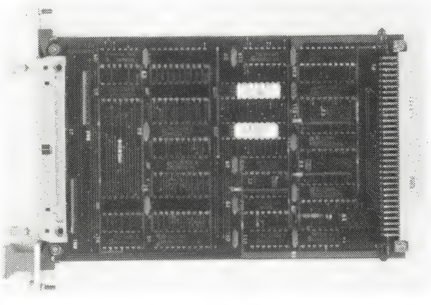
Board offers synchronous mode

Another product that serves high-speed, multithreading applications is the Model 300 VME host adapter from Introl. Model 300 not only works at the standard SCSI asynchronous transfer rate, but also transfers 4M bytes/sec in the synchronous mode. Upon start-up, Model 300 polls each device on the SCSI bus, identifies devices with synchronous capabilities, and communicates with them in the synchronous mode.

Model 300 uses a mailbox approach to command passing, but unlike other host adapters, it does not wait for the CPU to send a signal when a command block is ready. Rather, the host adapter circles through the command-block queue continuously, checking to see if commands are waiting. The system handles as many as 16 concurrent operations.

A Fujitsu MB87030 SCSI IC and controlling firmware manage the multimode operation of the Introl board. A 68000 µP controls the board, which also includes a 4k-byte buffer and a DMA controller. A version of the board uses differential bus tranceivers. Introl plans to supply a sample Unix driver with the board.

Use of the SCSI protocol is but one approach to system configuration. Proponents of device-level interfaces argue that true high-end systems—incorporating, for example, a 68020 µP and a 500M-byte Winchester hard disk—will not use the SCSI standard. (For a comparison of the SCSI with other interface standards, see the box in **Ref 1.**) Still other applications may benefit from a mixture of SCSI and other peripheral interfaces.



You can add SCSI capabilities to a VME system *for less than $200 with Mizar's VME8500, which appears as two read-only and two write-only registers to the VME Bus.*

The $1850 (1000) V/ESDI 4201 Panther from Interphase is one such combination board. It includes interfaces conforming to the SCSI and the Enhanced Small Device Interface (ESDI) standards. ESDI operation offers greater control over disk drives, to eliminate the rotation and command latency that's still common in SCSI operation. In the V/ESDI 4201, the ESDI circuitry supports four disks operating at rates to 20M bps.

Interphase expects that designers will use the SCSI port simply as an interface to a tape drive, but the Panther still provides a full-featured SCSI implementation. The board includes the Fujitsu SCSI IC, a DMA controller, and single-ended or differential tranceivers. Interphase offers I/O drivers for a variety of Unix-type operating systems.

For Multibus II systems, you can buy a host-adapter board that combines the Storage Module Device (SMD) disk interface and the SCSI. The $3725 Rimfire 2200 from Ciprico implements the SCSI port primarily for tape backup. The board carries a high price because of the high-performance SMD interface and the interface to Multibus II.

The lack of specialized ICs for a Multibus II interface has stunted the bus's potential growth. The bus-interface ICs from Intel are slowly appearing, and that should inspire the introduction of more Multibus II products. The SCSI bus should work well with Multibus II, because both standards promote the idea of distributed intelligence. You may expect to see Multibus II host adapters for the SCSI bus in the first half of 1987.

Indeed, more SCSI host adapters will emerge for all buses in the next year. You can even expect the SCSI to have an impact on the personal-computer market; many personal-computer users will retrofit the SCSI bus for computer I/O, and others will combine the SCSI bus with the IBM PC bus for industrial applications. To help you keep current on the availability of SCSI products, several companies issue guides (**Refs 2, 3,** and **4**). These companies update the guides every six months. **EDN**

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1. Wright, M, "SCSI ICs simplify I/O-bus configurations, but options entail extra design effort," *EDN*, September 18, 1986, pg 97.
2. *The SCSI source guide*, Technology Forums Ltd, 1986 (3425 Pomona Blvd, Suite F, Pomona, CA, 91768).
3. *The SCSI report*, Peripheral Concepts Inc, 1986 (18003-G2 Skypark Circle, Irvine, CA, 92714).
4. *VMEbus compatible products directory*, Vita, 1986 (10229 N Scottsdale Rd, Suite E, Scottsdale, AZ, 85253).

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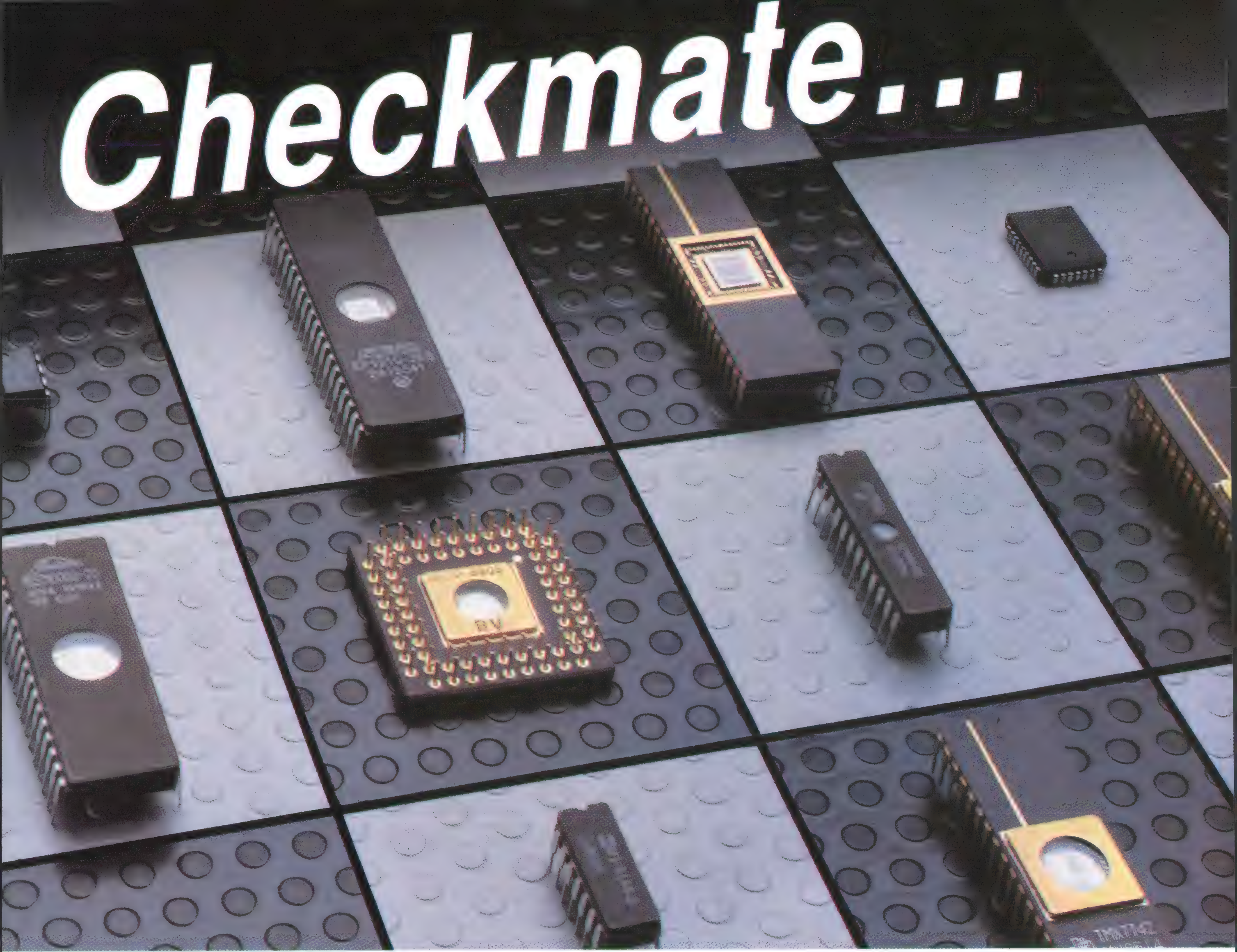

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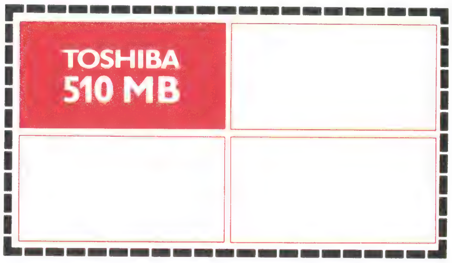

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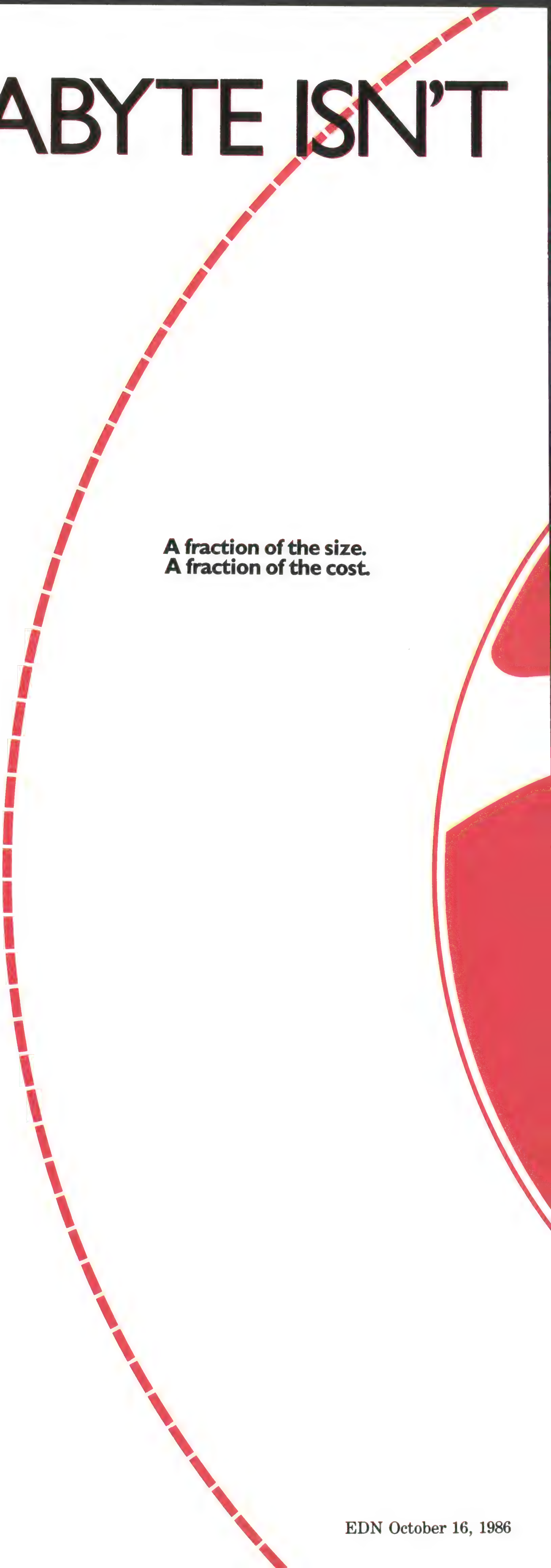
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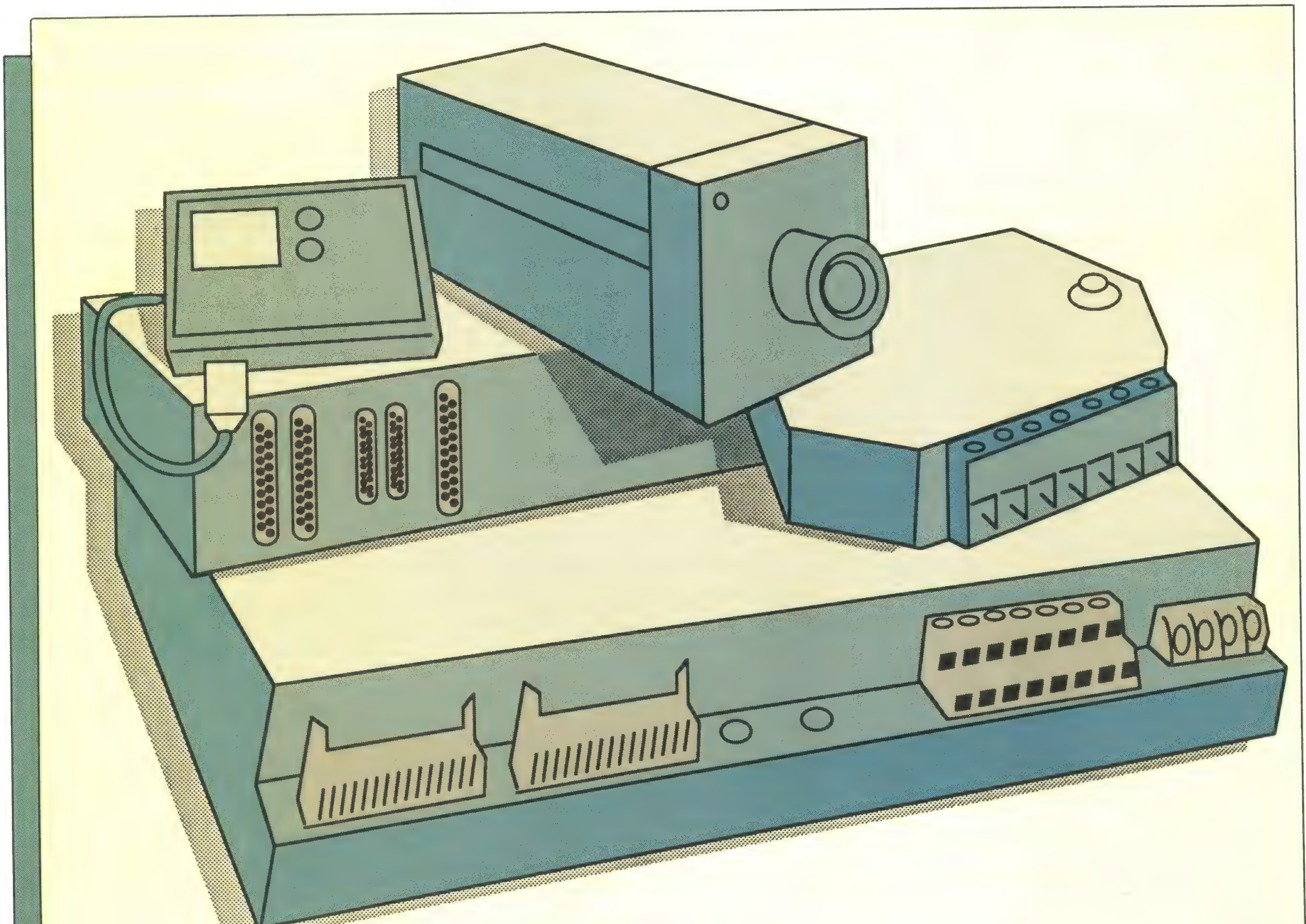

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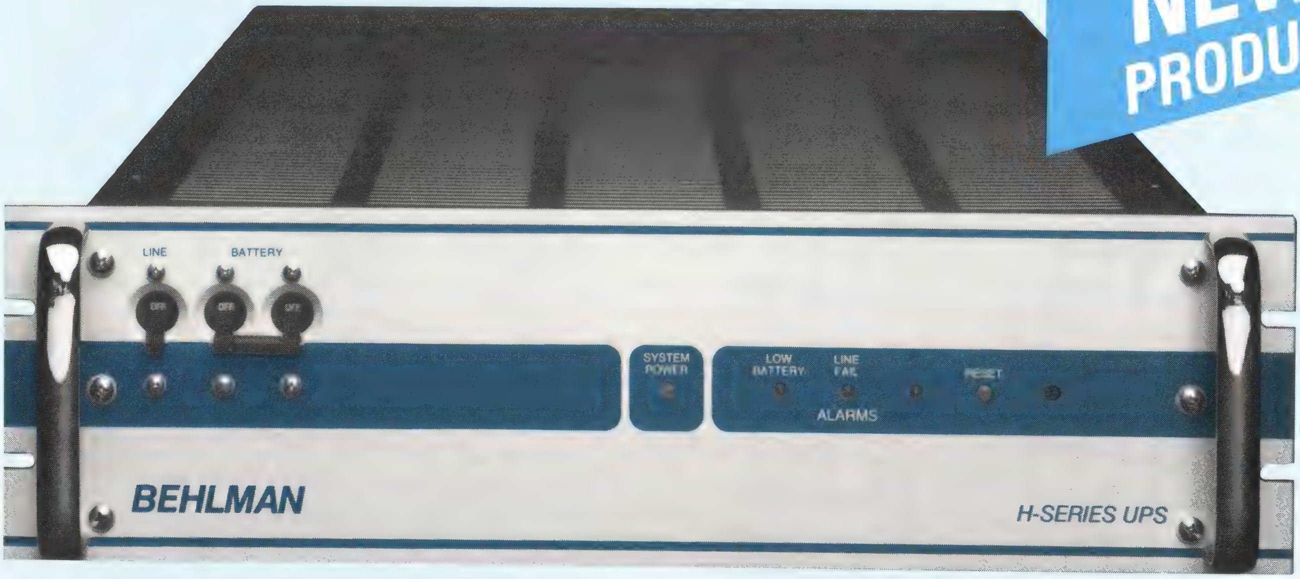

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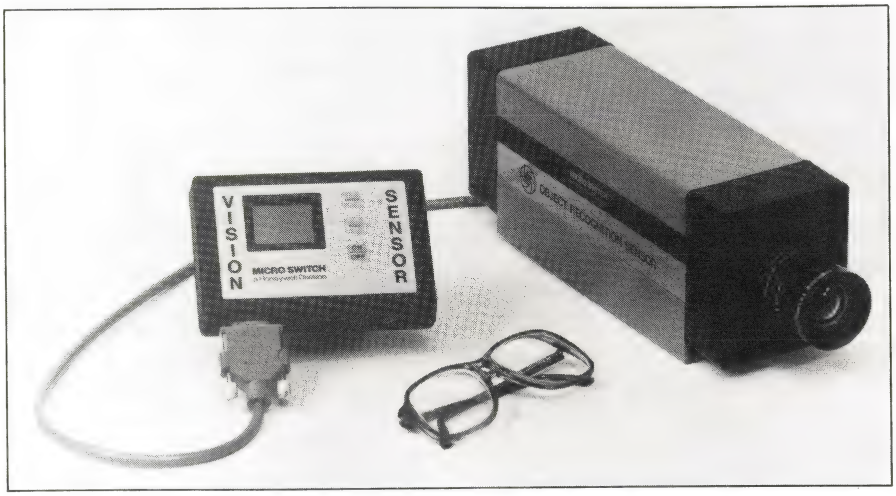

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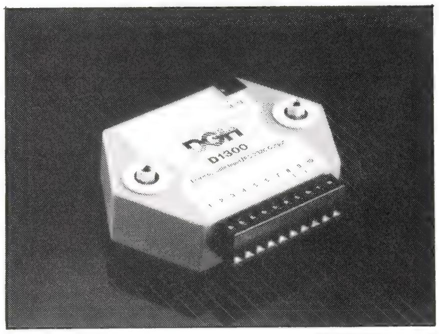


Offering analog-input-signal conditioning, A/D conversion, and on/off control features, D1000 Series data-acquisition and -control modules let you easily interface analog sensors to any computer that has a serial port. All 46 models (voltage, current, thermocouple, RTD, bridge, frequency, pulse, and digital) have RS-232C- or RS-485-compatible outputs.

The modules use an 8-bit μC to perform all scaling, linearization, and calibration tasks in software, so you don't need potentiometers, switches, or adjustment hardware. Every model has digital I/O lines, which permit on/off control of devices via solid-state relays or TTL signals.

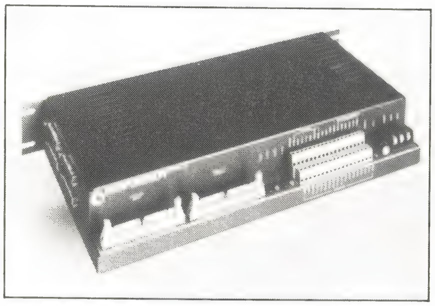
The command set is designed for measurement and control tasks. It tells the module to read data, alarms, and digital inputs; count events; establish a setpoint; set alarms; set digital outputs; and perform other functions. All command messages are preceded by a prompt and a channel address.

Communication features include channel address, baud rate (300 to 38.4k), parity, line feed, byte time delays, echo, and checksum. The modules store communications setups in nonvolatile memory. D1000 Series modules operate from one supply (10 to 30V) and draw 700 mW max. They operate over 0 to 70°C. $250 to $325.

DGH Corp, Box 5638, Manchester, NH 03108. Phone (603) 622-0452. TLX 510-601-6112.

Circle No 710

Industrial-strength microcomputer coordinates motion-control functions



The Model 52 industrial-control microcomputer is programmed in fast interpretive Basic and provides ready access to machine-language routines for I/O control. Nonvolatile memory accommodates program storage without the need for batteries or external memory devices. You can easily transmit programs into or out of the unit for editing or storage.

The system includes built-in real-time clock functions. It's housed in a NEMA-compatible enclosure and can be configured to run programs from power-on without operator input. You can program the μC via an external RS-232C terminal; after programming, you can remove the terminal, and the μC will operate as a stand-alone controller or computer.

Extensive I/O facilities are available. They include four RS-232C ports, eight optically isolated I/O lines, 48 I/O lines for use with signal-conditioning modules, analog input and output (A/D and D/A converters), counters/timers, and optical-encoder counting circuitry. The microcomputer is designed to operate at 50°C ambient temperature. $1750.

Compumotor Corp, 1179 N McDowell Blvd, Petaluma, CA 94952. Phone (800) 358-9068; in CA, (707) 778-1244.

Circle No 711

Programmable, 8-axis servocontroller suits space-limiting applications

In addition to providing eight axes of servocontrol, the Bam-8 can control and coordinate the nonservo functions of a machine or process. The servocontroller can accommodate as many as 512 industry-standard I/O devices to control relays, solenoids, lights, and other on/off devices.

The unit works with brush or brushless motors, PWM or linear amplifiers, and linear or rotary feedback encoders. It also works effectively with or without tachometers. Housed in a 13×9×3.5-in. package, the servocontroller easily fits into systems in which space considerations are critical.

Parasol II, the Bam-8's command language, is a complete motion-control and programming language that provides a unified approach to machine control and I/O operations. By using the servocontroller to control both motion and logic functions, you can eliminate programmable controllers, thus simplifying system development.

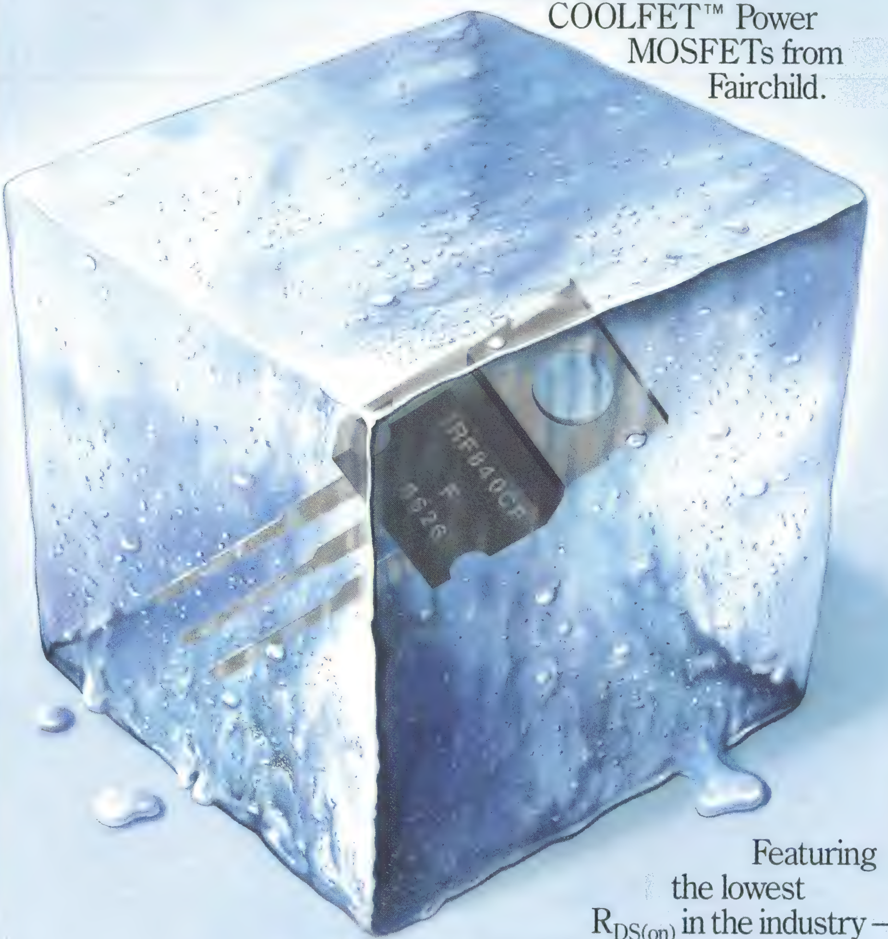
The controller features 100% digital design; 100k bytes of user memory; and RS-232C ports and IBM PC-compatible software for system setup, application-program development, and communication. Programs are written in Basic, C, and Pascal. $5995.

Berkeley Process Control Inc, 5327-K Jacuzzi St, Richmond, CA 94804. Phone (415) 526-3333.

Circle No 712

COOLFETs take the heat off Power MOSFETs.

When you're looking for Power MOSFETs that know how to beat the heat, look no further than the performance leaders: COOLFET™ Power MOSFETs from Fairchild.



Featuring the lowest $R_{DS(on)}$ in the industry – a full 20% lower. So you enjoy substantially less power loss, resulting in the coolest operation around. Which adds up to an increase in reliability and efficiency you simply can't find anywhere else.

Whether you use them as drop-in replacements or for new designs, COOLFETs provide higher performance with no price penalty. In new designs, they call for smaller heat sinks. So they take up less space, and deliver significantly increased power density.

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As with all Fairchild products, COOLFETs are backed by our extensive customer service and support. Including fast delivery. Excellent sample availability. And field technical specialists to provide any and all assistance you may need.

To order COOLFETs, simply add a CF suffix to your regular IRF MOSFET part number.

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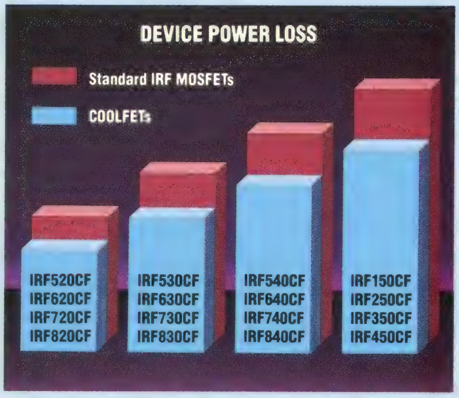

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CIRCLE NO 64

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For full information, write POWEREX, Inc., Hillis Street, Youngwood, PA 15697. Or call POWEREX headquarters at (412) 925-7272.

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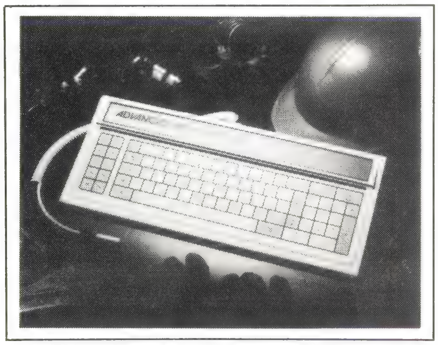
Joint Venture Corporation of Westinghouse, General Electric, and Mitsubishi.

CIRCLE NO 65



KEYBOARD

The PKD-83 IBM PC-compatible micromotion keyboard uses a sealed, gasketed top enclosure suitable for applications that must withstand heat, liquids, airborne contaminants, oil, and solvents. Incorporating a plastic overlay with embossed keys and standard legends, the keyboard is suitable for factory data collection and industrial process control.

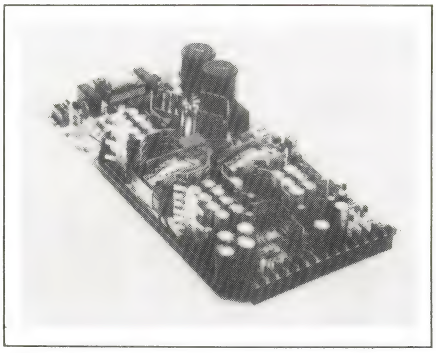
The keyboard uses snap-action, metal-dome key switches, which provide true-breakover tactile feedback. The keypanel's 83 positions include function keys, numeric characters and mathematical-function keys in a calculator-style arrangement, and separate cursor controls. The keyboard requires 5V at 200 mA max (150 mA typ). Its key travel measures 0.017 in.; typical actuating force is 11 oz. The keyboard operates over 32 to 140°F. $100 (OEM qty).

Advanced Input Devices, W 250 AID Dr, Coeur d'Alene, ID 83814. Phone (208) 765-8000. TWX 510-776-0584.

Circle No 689

SWITCHING SUPPLIES

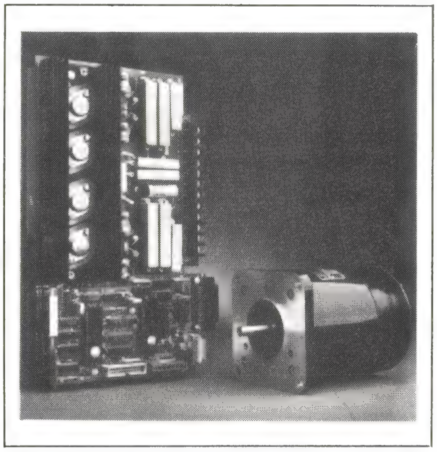
Maxi Series 350W open-board switchers provide five dc outputs: 5V/30A, 12V/10A, −12V/1A, 24V/5A, and −5V/0.1A. Load regulation is ±1% for the 5 and 12V outputs. The −5 and −12V outputs have linear postregulators that provide ±0.5% load regulation; the 24V output has ±5% load regulation. One channel, with its own switching transistor and transformer (operating at 30 kHz), provides the 5V output, and a second channel supplies the other four outputs. No cross regulation exists between the 5V output and the other four.



The switchers spec 75% efficiency, 32-msec holdup time, overload protection on all outputs, MOV-based transient protection on all inputs, overvoltage crowbar protection on the 5 and 12V outputs, and soft-start circuitry. The supplies meet FCC levels A and B radiation limits without requiring a shield or cover. They also meet FCC level B and VDE level A limits for conducted EMI. $525. Delivery, 4 to 12 weeks ARO.

Computer Products Inc, Boschert, 2900 Gateway Dr, Pompano Beach, CA 33069. Phone (305) 974-5500.

Circle No 690



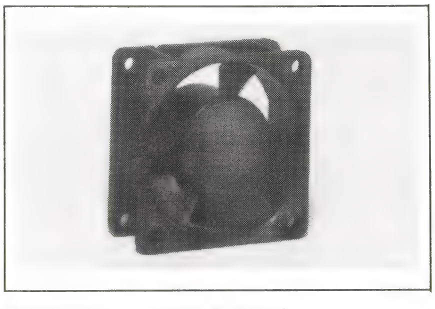
CHOPPER DRIVE

Designed to interface with stepper motors in process-control applications, this chopper translator board incorporates a MOSFET-output driver and proprietary resonance-compensation circuitry. Moreover, fewer parts on the board increase reliability. Half-step or 2ϕ on-stepping modes are switch selectable. The power drivers operate from unregulated supplies, and onboard DIP switches allow you to select one of 64 current levels.

Optional direct-mount digital and analog cards expand the translator board's capabilities. The digital card accepts ASCII-encoded commands over a 3-wire RS-232C interface; you can connect as many as eight units to one RS-232C port. The card also stores small, multiple-move programs for later execution, releasing the computer for other tasks. The analog card interfaces with relays, switches, and programmable logic controller systems. You can select stepping rate with onboard potentiometers, or use voltage-level control inputs. From $436.

Bodine Electric Co, 2500 W Bradley Pl, Chicago, IL 60618. Phone (312) 478-3515.

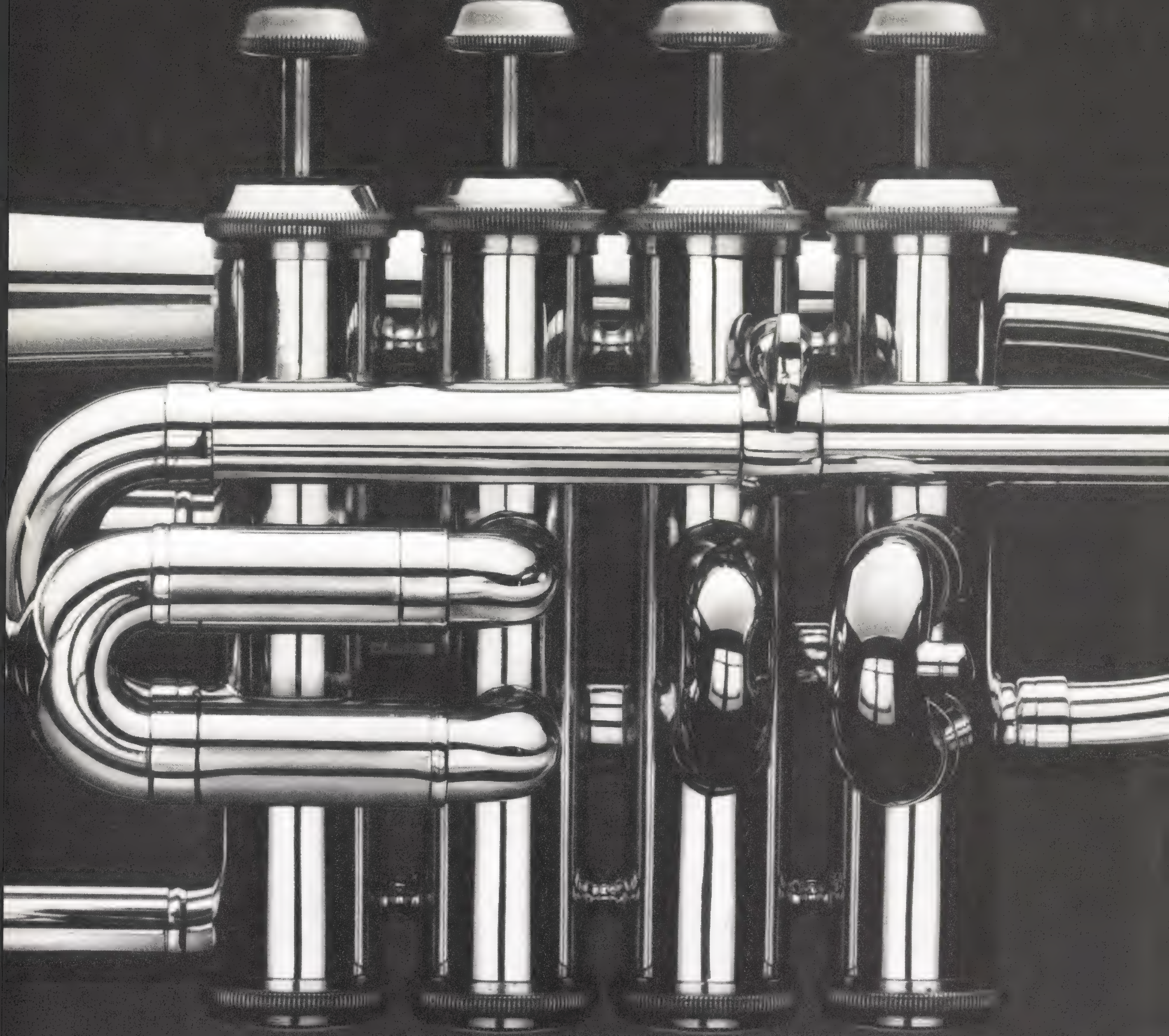
Circle No 691



BRUSHLESS FANS

These 2.5×2.5×1-in. brushless dc fans deliver 12 cfm of airflow at nominal input voltages of 12 or 24V dc (P0012-12D-2B and P0012-24D-2B, respectively). You can increase or decrease airflow by merely elevating or lowering the input voltage within its allowable range (8 to 15V and 16 to 30V, respectively). Because they are self-contained and require no external inverters, the fans are well suited for use in applications where mounting space is restricted. A high-precision ball-bearing system extends operating life:

If you're looking for all the latest bells and whistles...



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The fans last 50,000 hours at 60°C. They have a polycarbonate housing and impeller, wire leads, and polarity and locked-rotor protection, and they conform to UL, CSA, IEC and VDE safety standards. Approximately $10 (OEM qty).

Interfan, Box 4188, Burlingame, CA 94011. Phone (415) 347-1203. TWX 910-374-2353.

Circle No 692

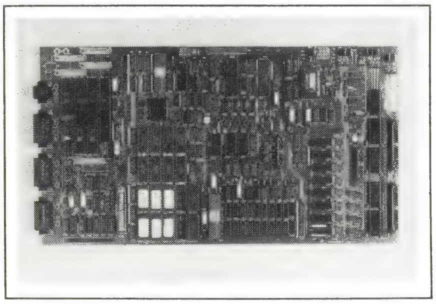
PROTOTYPE SYSTEMS

The STD-DOS PS 1.2 and OS 1.2 prototyping systems, employing various software tools, let you use an IBM PC or compatible to develop, test, and debug code; you can then download and execute that code on the STD Bus.

PS 1.2 includes six STD Bus cards (a multifunction 8088 CPU card, four memory cards, and an extender card), three system-support disks, a card cage, a power supply, and cabling. This complete system connects to a PC without requiring any modifications, and it allows you to do custom programming on the STD Bus. It will also accommodate various STD Bus I/O cards to satisfy specific applications. OS 1.2 includes a multifunction 8088 CPU card, two memory cards, and three software diskettes. It will run any application developed with PS 1.2. Both configurations include MS-DOS user license. PS 1.2, $2895; OS 1.2, $1480.

Pro-Log Corp, 2560 Garden Rd, Monterey, CA 93940. Phone (408) 372-4593. TWX 910-360-7082.

Circle No 693



CONTROLLER

The Sentinel, a 16-bit 80186/8087-based controller, integrates analog and digital I/O, pulse accumulation, and frequency inputs through built-in software—a PROM-based real-time OS and an enhanced Basic language (Dabil) that's optimized for process control. A dual-floppy-disk controller, battery-backed real-time clock and RAM disk, and four serial ports are standard. The controller's data-acquisition rate can reach 10,000 samples/sec. It accommodates RS-232C, RS-422, and RS-423 interfaces as well as a 250k-bps standard LAN.

True multiprocessing simultaneously manages dozens of independent processes, so you can cleanly divide complex applications into manageable subtasks. Dabil's long variable names and statement labels help you create self-documented programs, and incremental compiling accelerates program execution. Simple commands allow you to specify input gain and conversion and also provide automatic cold-junction compensation and linearization for thermocouples. $4500. Delivery, 60 days ARO.

Compudas Corp, Box 4688, Ithaca, NY 14852. Phone (607) 257-3003.

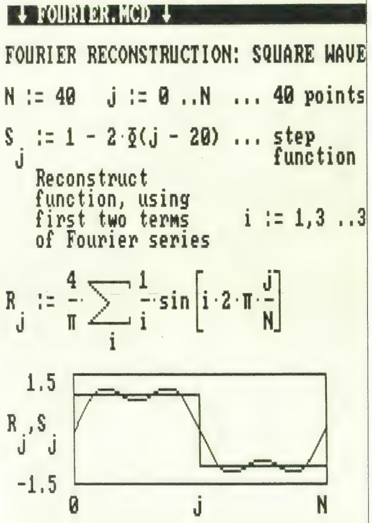
Circle No 694

MULTIBUS CHASSIS

The Series IV chassis features a 150W supply, a 4-position card cage with slots on 0.60-in. centers, and a cooling system. The system meets UL and CSA safety regulations and FCC standards for RFI/EMI. The removable front panel allows access

MathCAD

The Engineer's Scratch Pad



FOURIER.MCD

FOURIER RECONSTRUCTION: SQUARE WAVE

$N := 40 \quad j := 0 \,..\, N$ ... 40 points

$S_j := 1 - 2\cdot\Phi(j - 20)$ ... step function

Reconstruct function, using first two terms of Fourier series $\quad i := 1,3 \,..\, 3$

$$R_j := \frac{4}{\pi}\sum_i \frac{1}{i}\sin\left[i\cdot 2\cdot\pi\cdot\frac{j}{N}\right]$$

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Cambridge, Massachusetts 02139

CIRCLE NO 67

DIGITAL SIGNAL PROCESSING

ST-1172A Number Controlled Oscillator

This 2µ CMOS device enables significantly higher operating frequencies than ever before available for a monolithic direct digital synthesizer.

Features: 32-bit frequency resolution, parallel sine and cosine outputs, 25-MHz clock frequency, microprocessor bus compatible, low power consumption.

Applications: Frequency synthesizers, hi-speed frequency hopped sources, single sideband converters, digital signal processors, baseband receivers.

STI-2003 Complex Multiplier/Accumulator

The CMAC is well suited for demodulation of digital data in satellite communication links. The complex multiplication function on one chip offers single chip solutions to special signal processing tasks.

Features: 4-bit resolution, 22-bit accumulator, latched overflow and underflow bits, maximum multi-accumulate rate of 6 MHz, 8-bit processor bus interface, on-chip address latch, completely TTL compatible, very low power consumption.

Applications: Digital demodulators, digital image rejection mixers, adaptive equalizers, digital matched filters.

STI-5268 Convolutional Coder/Viterbi Decoder

Provides forward error correction (FEC) to improve digital communication performance over a noisy link. Where transmission power is limited, FEC techniques can reduce the required transmission power.

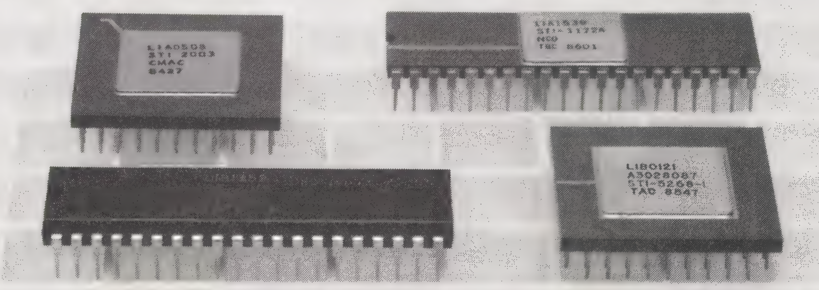
Features: Constraint length 7, rate 1/3 or 1/2, 3-bit soft decision in sign magnitude of 2's complement format, up to 9600 bit/sec data rate, both encoding and decoding functions performed, extremely low power consumption.

STI-2010 Viterbi Decoder

Provides forward error correction in higher data rate links where the flexibility exists to use a constraint length 6 code.

Features: Constraint length 6, rate 1/2 or 1/3, 4-bit quantization input, internal node sync, on-chip memory, up to 256K bits/sec data rate.

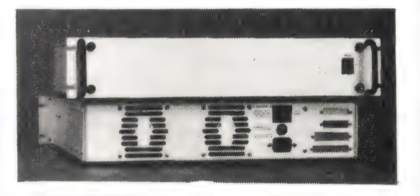
For further information, call or write:
Stanford Telecommunications, Inc., (Attn: Patti Laakso), 2421 Mission College Blvd., Santa Clara, CA 95054-1298 (408-980-5684)



SOLUTIONS

STANFORD TELECOMMUNICATIONS

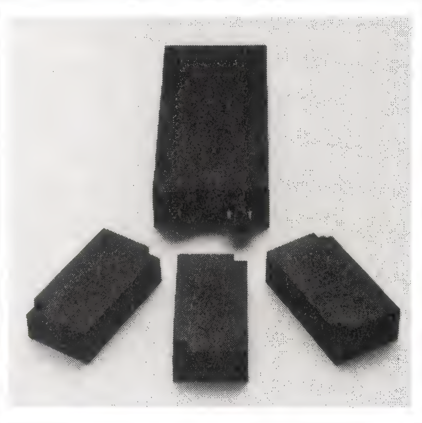
CIRCLE NO 68



to the system cards, and the rear panel has an on/off power switch and cutouts for four D-type connectors. All P1 system bus lines are traced and terminated per IEEE-796 standards. P2 auxiliary connectors are optional. The quasiregulated supply offers four high-current outputs, and two 3⅛-in.-square fans provide cooling by forcing air in a precisely guided flow pattern over the power supply, card cage, and through the vented top cover. $1195.

Chen Digital Laboratories, 4170 148th Ave NE, Redmond, WA 98052. Phone (206) 881-5031.

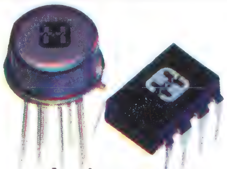
Circle No 695



R/W SYSTEM

Two modules, the encapsulated Model 8000 reader/writer and the Model 2000 tag, together provide null-free operation in an 8k-byte RF read/write system. The system ties into a host computer or programmable controller via an RS-232C, RS-422, or 4- to 20-mA current-loop interface and a simple user protocol. Because it uses low-frequency radio waves, the system avoids the problems associated with microwave-RF systems. It has a well-defined RF field and an increased ability to read through contaminated environ-

Give your industrial controls a lift with our high-performance analog ICs.



When you put industry-proven Harris linear and data acquisition ICs into your control designs, you always come out ahead — in design time, cost, and product performance.

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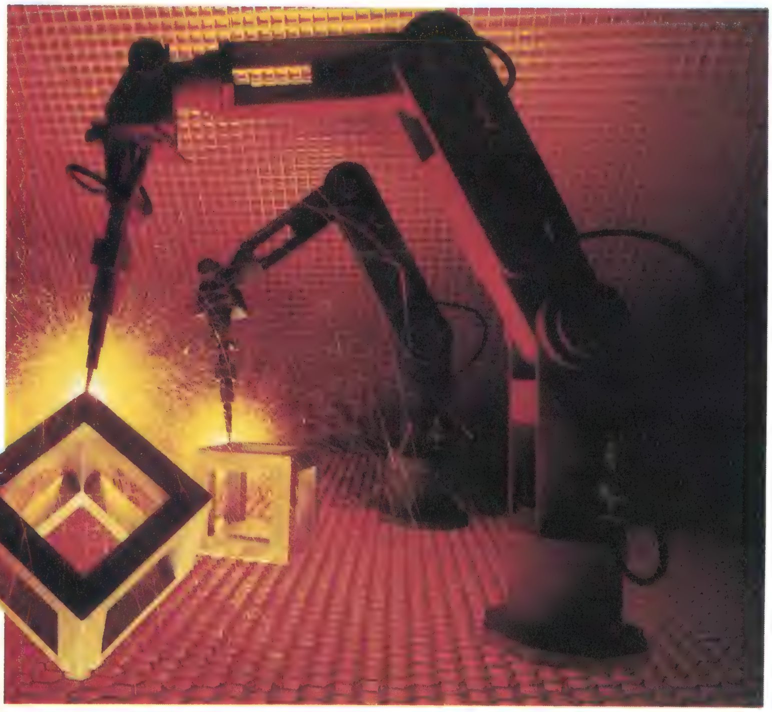
For data acquisition, choose our A/D and D/A converters, sample-and-hold amplifiers, and analog multiplexers.

Our Dielectric Isolation (DI) process means no latch-up, plus higher speed and performance characteristics.

Get Harris into your system.

Contact: Harris/MHS Semiconductor Sales Ltd., Eskdale Road, Winnersh, Wokingham, Berks, RG11 5TR, England.

We'll help handle your load.



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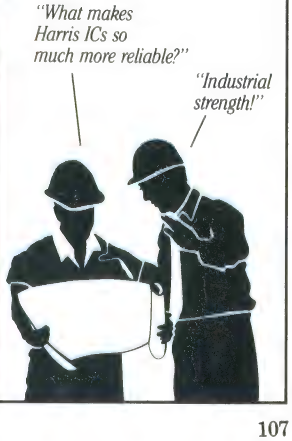

"What makes Harris ICs so much more reliable?"
"Industrial strength!"

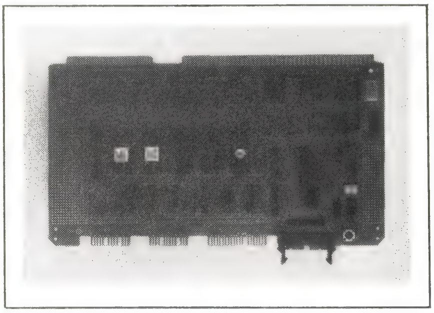
CIRCLE NO 69

ments, and it poses no health hazards.

You can program the FCC-certified system to handle scanning distances ranging to 2 ft. Model 8000, $1800; Model 2000, $95. An evaluation kit, containing one reader/writer module, two tag modules, a cable for connection to an IBM PC or compatible, driver software, and source code is available for $1950. Delivery, stock to six weeks ARO.

Escort Memory Systems Inc, 1 Victor Square, Scotts Valley, CA 95066. Phone (408) 438-7001.

Circle No 696



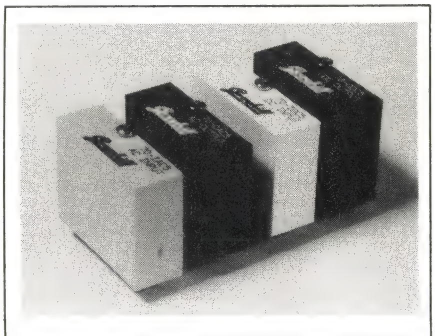
MOTOR CONTROLLER

The DMC-205 is a single-axis, dc motor controller that synchronizes motion with an external master frequency. It will accept the master-frequency input in two formats—as a pulse train or as encoder pulses in quadrature.

You can program the upper limit of the master frequency, which falls within the 128- to 250,000-Hz range. During master/slave operation, the controller monitors the actual master frequency, and computes the ratio between the master and specified maximum frequencies. It then scales the slave's slew speed and acceleration by the ratio and square of the ratio, respectively. You can program motion commands and control parameters using the Multibus or the RS-232C interface. An on-board μP executes the control algorithm every 1 msec. $1295.

Galil Motion Control, 1928-A Old Middlefield Way, Mountain View, CA 94043. Phone (415) 964-6494.

Circle No 697

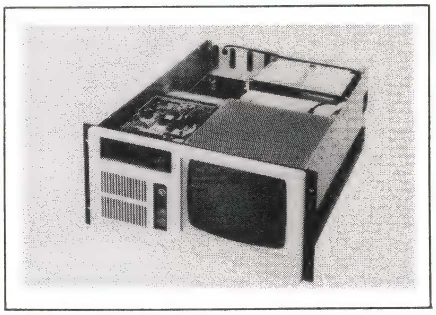


I/O MODULES

Series 70 I/O modules (ac and dc output, ac and dc input) feature 4000V isolation protection of the logic circuitry. The modules' SMT design results in superior heat-transfer characteristics. AC-output modules operate with inputs of 5, 15, or 24V dc and can switch 120 or 240V ac loads. AC-input modules monitor 120 or 240V ac loads or sensors and provide corresponding 5, 15, or 24V dc signals to logic circuitry. DC-output modules switch 3 to 60V dc loads when operating with inputs of 5, 15, or 24V dc. DC-input modules monitor 3 to 32V dc loads or sensors and generate 5, 15, or 24V dc signals to logic circuitry. $6.20 to $8.17 (100).

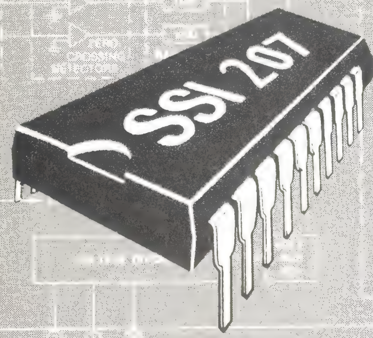
Grayhill Inc, Box 10373, La Grange, IL 60525. Phone (312) 354-1040. TLX 6871375.

Circle No 698



ENCLOSURES

Designed to house IBM PC/XTs or PC/ATs (or compatibles), Models RME-900 and RME-100 are 19-in. rack-mount enclosures offering EMI protection in industrial enviroments. They feature easy access to all cards, filtered air cooling, rear I/O connector panels, and 8-card ca-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INDUSTRY'S FIRST MONOLITHIC MF IC RECEIVER

FEATURES:
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- Detects all 15 tone pairs including ST and KP
- Long KP capability
- Outputs in either "n of 6" or hexadecimal code
- Built-in amplitude discrimination
- Excellent noise tolerance
- Single low-tolerance 5V supply
- Three-state outputs, CMOS-compatible and TTL-compatible
- 20-pin plastic DIP

Silicon Systems has introduced the industry's first monolithic multi-frequency (MF) receiver. Designated the SSI 207, this new chip for the first time allows the user to dramatically reduce the component space and power previously required by hybrid or board-level solutions.

Optimum for use in equal access applications, the SSI 207 meets Bell and CCITT R1 central office register signaling specifications. No anti-alias filtering is needed for input signals band-limited to 26kHz, and the only external component required is an inexpensive television "color burst" crystal.

For more information, contact: **Silicon Systems,** 14351 Myford Road, Tustin, CA 92680. **(714) 731-7110, Ext. 433.**

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CIRCLE NO 70

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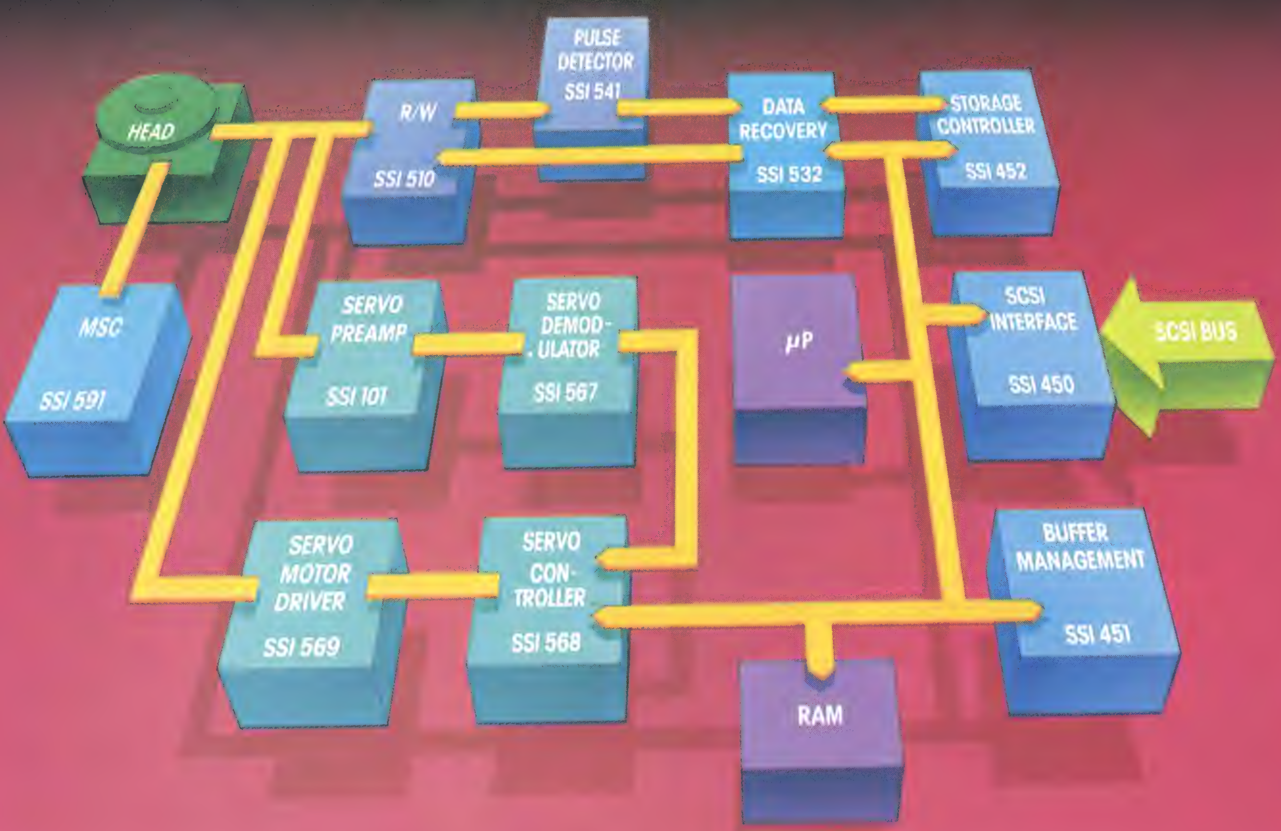

SCSI CHIP SET

New Chip Set Provides "Head-to-Host" Solution

The demand for higher capacity Winchester Disk Drives has led to Silicon Systems' introduction of a complete line of small computer system interface (SCSI) products. This exciting new line of 11 ASIC's for intelligent disk drives does it all. The chip set provides silicon solutions for the entire read channel, for the controller and interface electronics, for a dedicated surface-servo-head positioning system, and for spindle motor speed control.

Maximizes Functionality into Smallest Footprint

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Silicon Systems, 14351 Myford Road,
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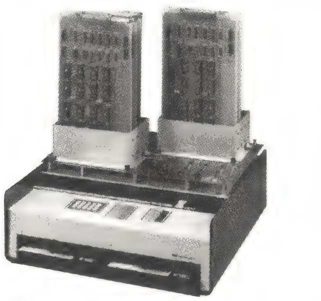
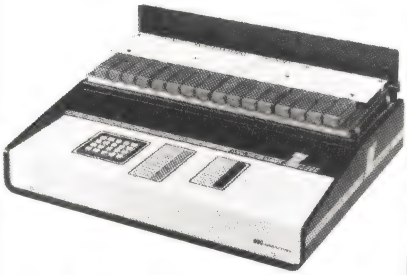


Z-2500B IN-CIRCUIT MEMORY CARD PROGRAMMER

- Programs and tests up to 32 customer memory cards populated with EPROMs or microcomputers at a time.
- Two 1.2 Mbyte DSDD floppy disk drives. Optional 20 Mbyte hard disk.
- Simple menu driven operation.
- Turnkey systems include programmer, terminal, custom interface hardware and software.



Z-3000 HIGH VOLUME GANG/SET PROGRAMMER

- 14,000 27256's programmed per day.
- 32 EPROMs simultaneously with 1 to 8 DATA BLOCKS.
- 16 Intel or Motorola MCUs at a time.
- 64K to 256K bytes of DATA RAM.

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Z-1000B UNIVERSAL PROGRAMMER

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CIRCLE NO 71

pacity. Model RME-900 includes a 9-in. monochrome monitor and provides mounting space for one full-height or two half-height hard-disk drives, and a half-height floppy-disk drive. Model RME-100 has no monitor but will accommodate combinations of floppy-disk drives, hard-disk drives, and tape backup. It has room for two full-height and two half-height 5¼-in. drives. RME-900, $625; RME-100, $495.

Recortec Inc, 275 Santa Ana Ct, Sunnyvale, CA 94086. Phone (408) 737-8441.

Circle No 699

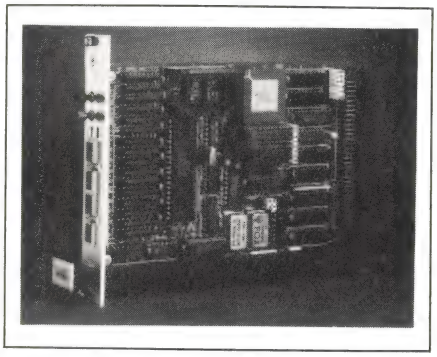
LEVEL CONTROL

The LCT 506-6200 Magi-Cal Series point-level control is a 2-wire transmitter for level indication of various process materials. Its 2-wire design ensures intrinsically safe operation, and the Magi-Cal pushbutton calibrator permits remote system calibration. The LCT electronic unit connects to a Series 700 sensing element, which is located in the vessel of the material being measured. When the material level reaches a preset point in the vessel, the transmitter provides a step change in its 4- to 20-mA output. Cote-Shield circuitry allows the transmitter to ignore the effects of material build-up on the sensing element.

Alternatively, you can use the electronic unit with 401-3700 Series TTL modules for interfacing to customer-supplied programmable controllers, computers, and annunciators, or with 401-3000 Series relay-output receivers. $600 to $870 for the sensing element, transmitter, and calibrator. Delivery, six to eight weeks ARO.

Drexelbrook Engineering Co, 205 Keith Valley Rd, Horsham, PA 19044. Phone (215) 674-1234.

Circle No 700



COMPUTERS

SBC1 Series single-board computers provide stand-alone VME Bus processing capability. Compatible software support includes the Microcraft Soft Emulator debug monitor, the Microware OS-9 OS, and the Alcyon Regulus real-time implementation of Unix V.2. The board contains a 10-MHz 68000 or 68010 μP, two serial ports with programmable baud rates (50 to 38.4k bps), a programmable counter/timer, sockets for 512k bytes max of local zero-wait-state dynamic RAM and 128k bytes max of EPROM, a VME Bus controller, and a 7-level interrupt handler that supports vectored and autovectored interrupts. The board is compatible with 3U and 6U form factors. $695.

VME Specialists, 558 Brewster Ave, Suite 1, Redwood City, CA 94063. Phone (415) 364-3328.

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8840A	$760	8842A	$995
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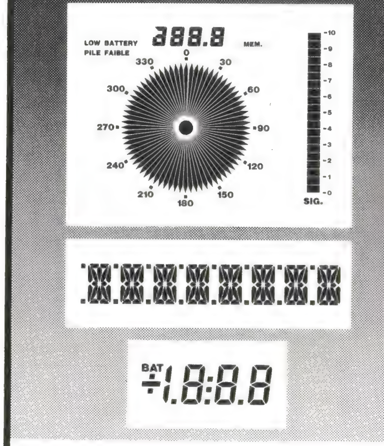

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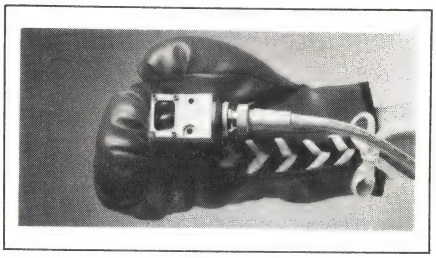
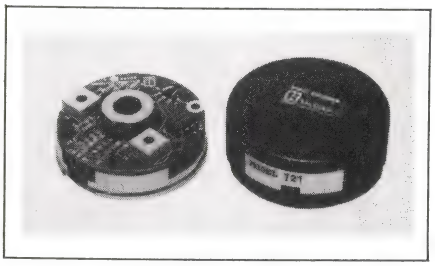


coupling simplifies installation. You can mount the sensor either flush on a flat surface using two mounting screws or by using the sensor's threaded base and mounting nut. Its visible light beam and its alignment-indicating device (AID) contribute to easy, accurate alignment. AID is a built-in system that shows both alignment and exact signal strength.

All scanner circuitry is epoxy encapsulated. The Valox housing is sealed and rated watertight according to NEMA-4 standards. You can choose from five scanning modes: retroreflective, opposed, diffuse, convergent, and fiber optic. Scanning capability ranges to 30 ft in the retroreflective mode and 200 ft in the opposed mode. $74.

Banner Engineering Corp, Box 9414, Minneapolis, MN 55440. Phone (612) 544-3164.

Circle No 702

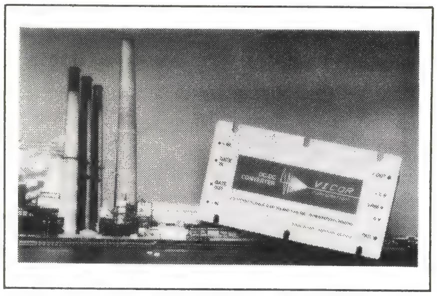


DIGITAL ENCODER

The Model 721 incremental modular encoder features self-alignment, automatic gap adjustment, a rugged metal base, and a snap-on cover. The encoder offers quadrature outputs (TTL/CMOS compatible), along with a marker pulse, and it's available with resolutions ranging to 1800 cycles. Operating frequency ranges to 100 kHz. Slewing speed is 6000 rpm max, and acceleration is 10^5 rads/sec^2. The encoder uses an LED illumination source that's rated for 100,000 hours min. Standard outputs range from 5 to 24V dc ±5% at 125 mA. A differential line driver is optional. The unit's cover meets UL 94V-0 requirements, and its shielded cable is UL/CSA approved. $35 (100).

Litton Systems Inc, Encoder Div, 20745 Nordhoff St, Chatsworth, CA 91311. Phone (818) 341-6161. TWX 910-494-1229.

Circle No 703



DC/DC CONVERTERS

VI-100-I Series converters offer power densities as high as 25W/in.^{3} Based on a 1-MHz, zero-current-switching forward-converter topology, the units achieve efficiencies of 80% min. Input-to-output isolation is 3750V ac. Designed to meet MIL-810 shock and vibration specifications, the modules feature logic disable, adjustable outputs, current limiting, and overvoltage protection. MTBF (per MIL-STD-217D) is 214,000 hours at 80°C. Specifications include 0.1% line regulation, 0.2% load regulation, 1% p-p output noise max (dc to 20 MHz), and 300-μsec transient response. $240.

Vicor Corp, 23 Frontage Rd, Andover, MA 01810. Phone (617) 470-2900. TWX 910-380-5144.

Circle No 704

PACKAGING SYSTEM

Express, a packaging system based on VME and DIN specifications, includes prototype panels that use SMT decoupling capacitors, card cages, backplanes, 100-kHz switching supplies, extender boards, and SMT adapters.

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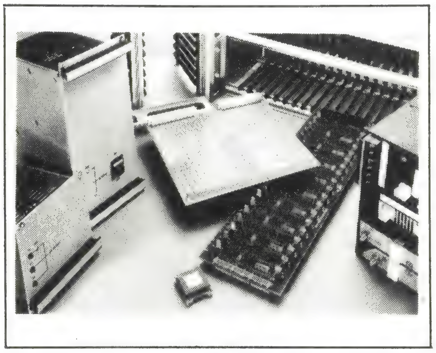
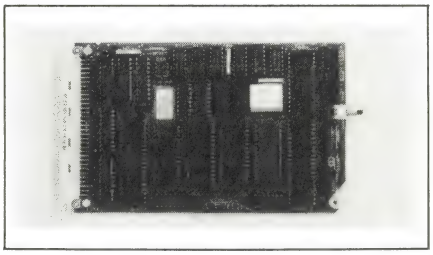


The Fastpak prototype panels feature 0.1-μF decoupling capacitors positioned under each IC. The ratio of decoupling capacitor to IC is 1:1, suiting the panels to high-speed applications. Designed for VME systems that use a 20-MHz clock, the backplanes offer 6-layer construction and large ground planes, reducing crosstalk by a factor of 2:1 when compared with 4-layer panels. The Extender boards use a 4-layer, controlled-impedance construction; two connector locations on each board let you monitor all signals with a logic analyzer. A system that includes a rack-mountable, 6U×160-mm-deep, 20-position card cage and a 20-position J1 backplane costs $556.50.

Augat Inc, Interconnection Systems Div, Box 1037, Attleboro, MA 02703. Phone (617) 222-2202. TWX 710-391-0644.

Circle No 705



CMOS COMPUTER

The RM65-1100 single-board computer provides 32k bytes of memory and RS-232C and VIA I/O ports. Based on a 2-MHz version of the CMOS 65C02 CPU, it includes a 65C51 ACIA device and a 65C24 VIA device, which provide the RS-232C port with onboard baud generation, two additional 8-bit ports, four control ports, and one or two 16-bit timer/counters. The module also includes four 28-pin sockets for as much as 32k bytes of PROM/RAM/ROM byte-wide devices; one socket will accept the company's 24-pin language ROMs (Forth, Basic).

The computer features onboard decoding and bank switching. Bank decoding and DMA terminate-control are optional; bank decoding will accommodate as much as 128k bytes of memory. With 8k bytes of memory, $245.

Dynatem Inc, 19 Thomas, Irvine, CA 92718. Phone (714) 855-3235. TWX 910-595-2603.

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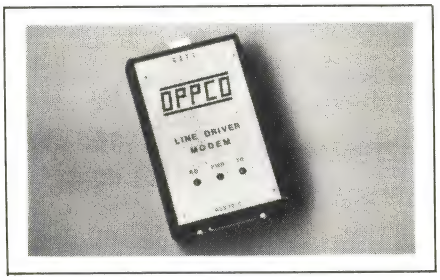

LINE DRIVER

The OP-3A, a self-contained line-driver modem, permits full-duplex data communications over long distances: 19.2k baud over 5 miles, or 250k baud over 2.5 miles. It operates from 110V ac, and its error rate is less than 1 in 10 billion bits. Three LED indicators simplify data-link troubleshooting. Using internal switch options, you can essentially augment any RS-232C DCE (data-communications equipment) or DTE (data-terminal equipment) configuration without modifying the system cable. The standard modem includes a power supply, but you can opt to use your own power source (12V at 120 mA, and −12V at 15 mA). $119 with supply; $97 without. Delivery, two to eight weeks ARO.

Oppco, 6407 S Kline St, Littleton, CO 80127. Phone (303) 978-1681.

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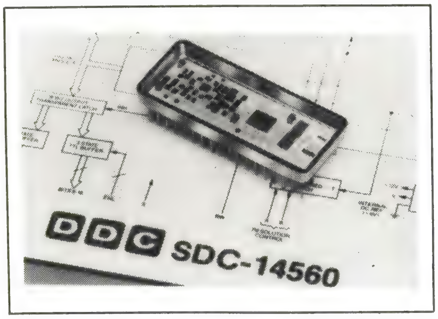

S/D CONVERTERS

The SDC-14560 Series synchro- or resolver-to-digital converters have a user-programmable resolution of 10, 12, 14, or 16 bits, and include a velocity output. You can obtain precise positioning by operating the converters in the 16-bit mode; the 10-bit mode provides fast tracking. The active-selection design allows you to change resolution without interrupting system operation.

The output is a 0 to ±10V ground-based voltage that's positive for increasing angles; this output allows you to close a velocity loop without employing a tachometer. The units accept broadband inputs of 360 to 1 kHz or 47 to 1 kHz. Their 3-state, digital angle output is a natural binary code that's TTL/CMOS compatible. Two operating ranges are available: 0 to 70°C and −55 to +125°C. From $345. Delivery, three months ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

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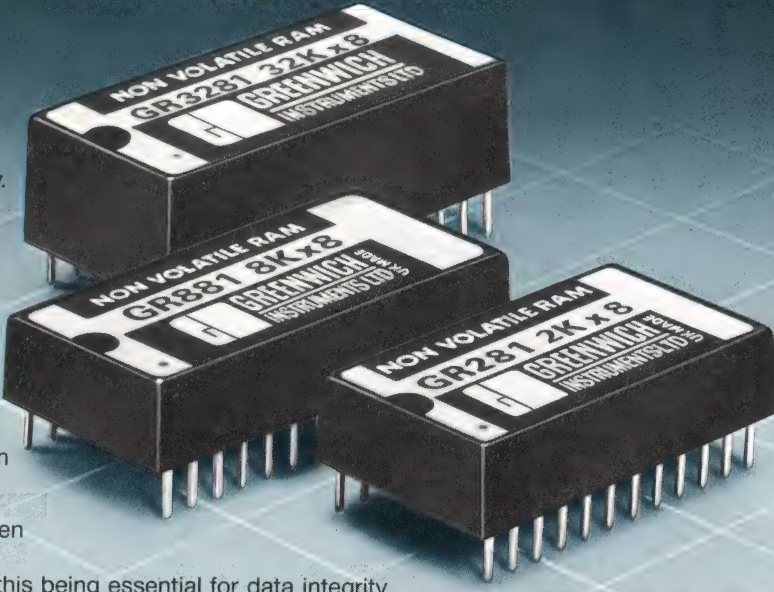

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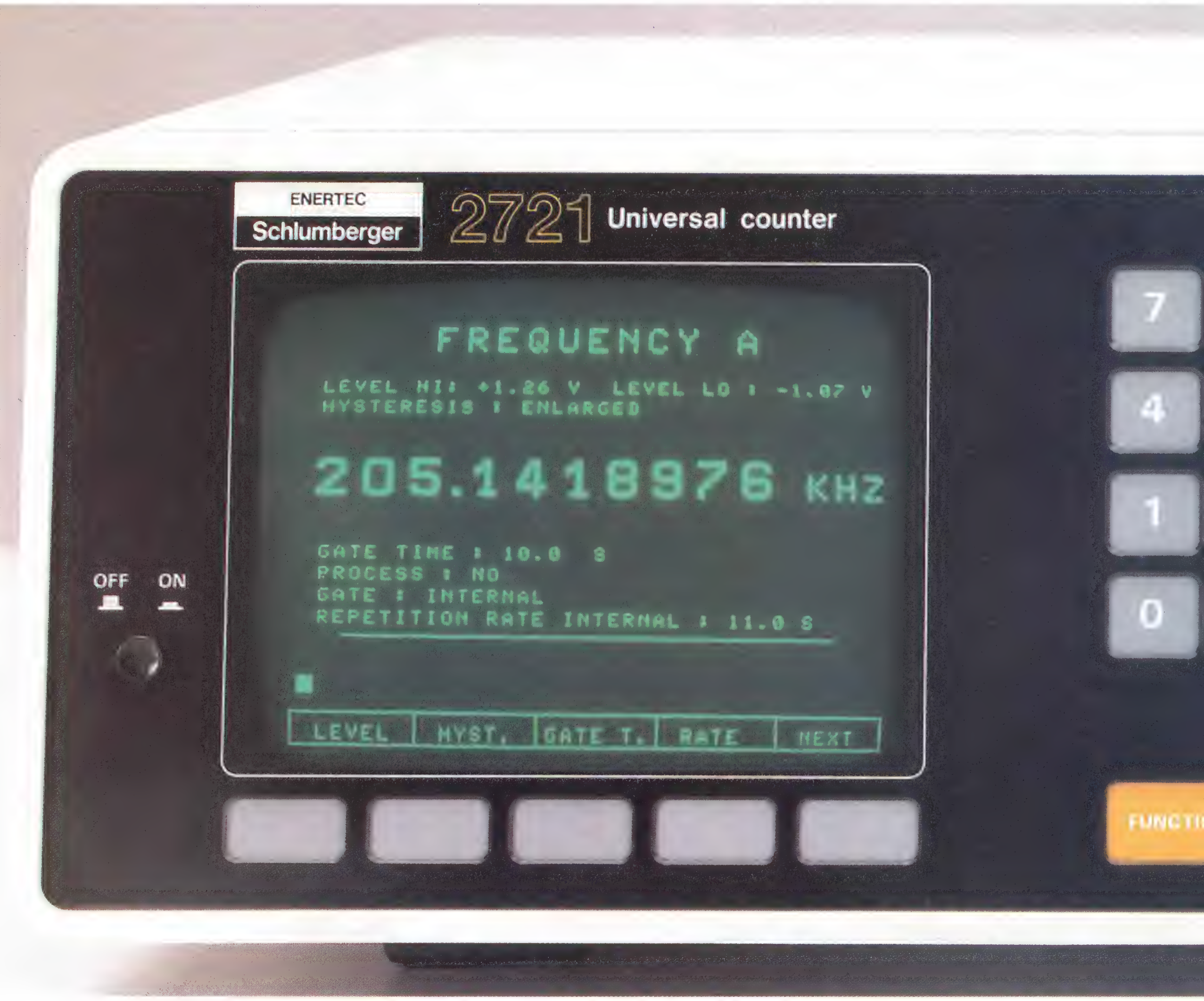

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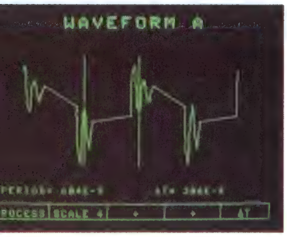

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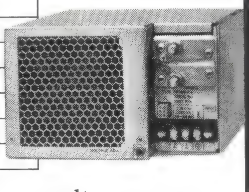

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Digitizing architecture is making scopes easier to use, and more efficient.

The move toward digitizing architecture in oscilloscopes is on. New digitizing scopes are easier to use, and can dramatically boost measurement efficiency for engineers and technicians in many applications.

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With conventional scopes, making measurements such as risetime or frequency is typically a lengthy process, involving manual calculations. With the HP 54000 series, you can make these measurements, and many more, automatically. That's because they are computed for you at the touch of a button from digitized information.

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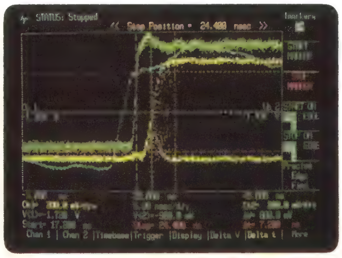

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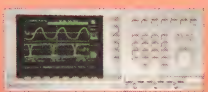


hp HEWLETT PACKARD

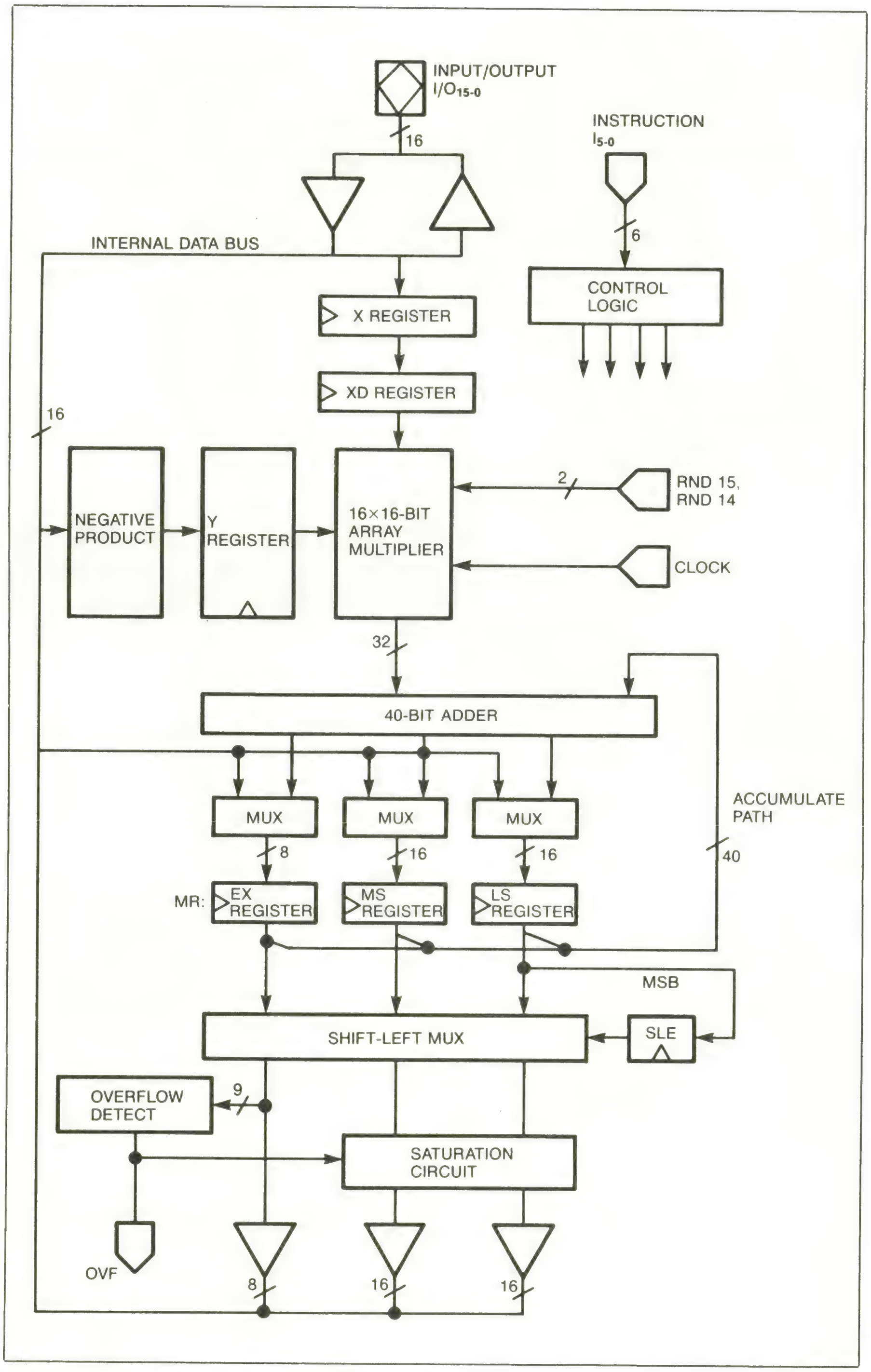
Single-port multiplier/accumulator IC has >10-MHz computational bandwidth

A high-speed, low-power, single-port multiplier/accumulator IC, the ADSP-1110A offers processing throughput comparable to that of existing 3-port devices. The ADSP-1110A's single-bus structure minimizes the pin count—the IC comes in a 28-pin plastic or ceramic DIP or in a 28-pin PLCC. The single bus also makes it easy for you to interface the IC to single-bus peripheral devices. Like its predecessor (the 190-nsec ADSP-1110), with which it is pin compatible, the ADSP-1110A uses CMOS processing for low (150-mW) power dissipation.

All inputs to and outputs from the ADSP-1110A pass through the IC's single 16-bit I/O port. All I/O operations are of the single-cycle type. You need two cycles to complete a multiply or multiply/accumulate operation (you need two cycles to load input pairs into the multiplier). An input pipeline register lets you load a new pair of inputs during the computation of a previous multiply/accumulate operation. The IC's pipelined throughput is therefore equivalent to that of larger, more expensive multiplier/accumulators.

The pipeline feature allows the device to attain computational bandwidths corresponding to its specified maximum multiply/accumulate time—85, 100, or 130 nsec, depending on grade. A 6-bit microcode instruction word governs the IC's operation. The instruction set focuses on I/O and multiply/accumulate operations; additional instructions allow you to obtain extra resolution in single- and double-precision operations.

The shift-left-on-output control, for example, scales up the outputs of the MR (multiplier result) register bank by a factor of two. This func-



The ADSP-1110A's single I/O port minimizes the IC's pin count and makes it easy for you to interface *the device to peripheral components. The unit has more than twice the speed of its manufacturer's earlier ADSP-1110. The 40-bit multiply register allows the IC to accumulate as many as 256 32-bit products.*

tion is useful in 2's-complement multiplication, which typically results in redundancy in the two most significant bits of the 32-bit product. The shift-left feature lets you obtain full precision in 2's-complement operations. The shift-left control also maximizes resolution when you're using block floating point and when you're shifting mixed and unsigned-magnitude results one bit left.

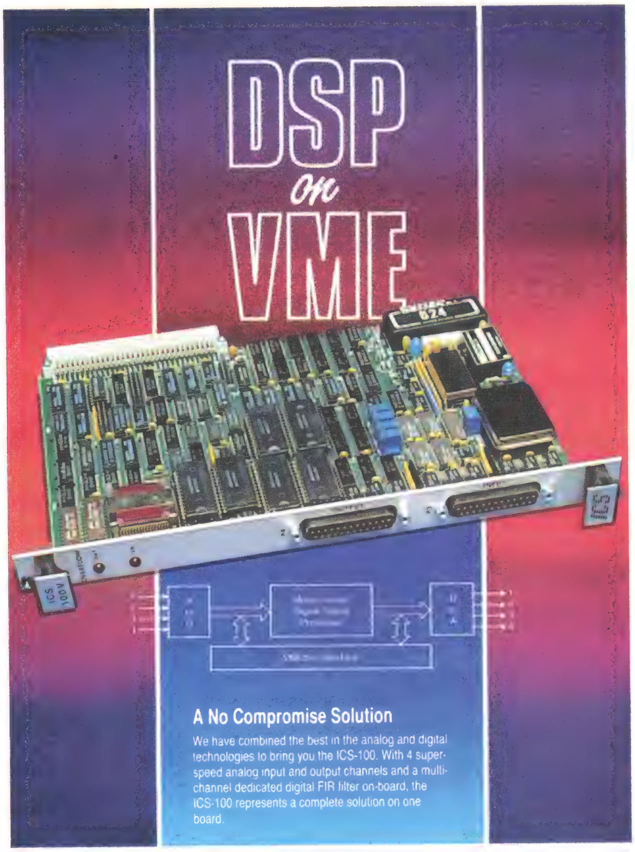
The pins RND_{14} and RND_{15} are two independent controls that allow for rounding-off operations consistent with shifted or unshifted operations, respectively. When you assert one of the RND controls, the IC adds a logical one to bit 15 or 14 of the lower 16-bit portion of the 32-bit product.

The 40-bit multiply register accumulates as many as 256 32-bit products. The IC provides for external monitoring of overflow bits from the MR's lower 32 bits into the 8-bit extension register. The ADSP-1110A can, depending upon overflow status, saturate the MR's outputs to full scale.

The ADSP-1110A is available with an operating-temperature range of either 0 to 70°C or −55 to +125°C. Prices range from $37 (100) for the commercial-range ADSP-1110AJN (in a plastic DIP) to $155 for the MIL-screened ADSP-1110ATD/883B (in a hermetic, ceramic DIP).—***Bill Travis***

Analog Devices Inc, Box 280, Norwood, MA 02062. Phone (617) 329-4700.

Circle No 732



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CIRCLE NO 83

Single-chip hard-disk controller supports DMA, dual-sector interleave

Capable of controlling any combination of four floppy- or hard-disk drives, the Model Am9580 VLSI disk-controller IC contains on-chip error checking, dual-sector buffers, and direct memory access (DMA). The chip provides three error-checking schemes: cyclical redundancy check (CRC, for detection only) and single- and double-burst Reed-Solomon error detection and correction.

According to the manufacturer, the error detection and correction provided by the Reed-Solomon schemes is three to four times more reliable than that provided by traditional fire codes. In addition to having better single- or double-burst capabilities, the Reed-Solomon codes have a smaller probability of miscorrection.

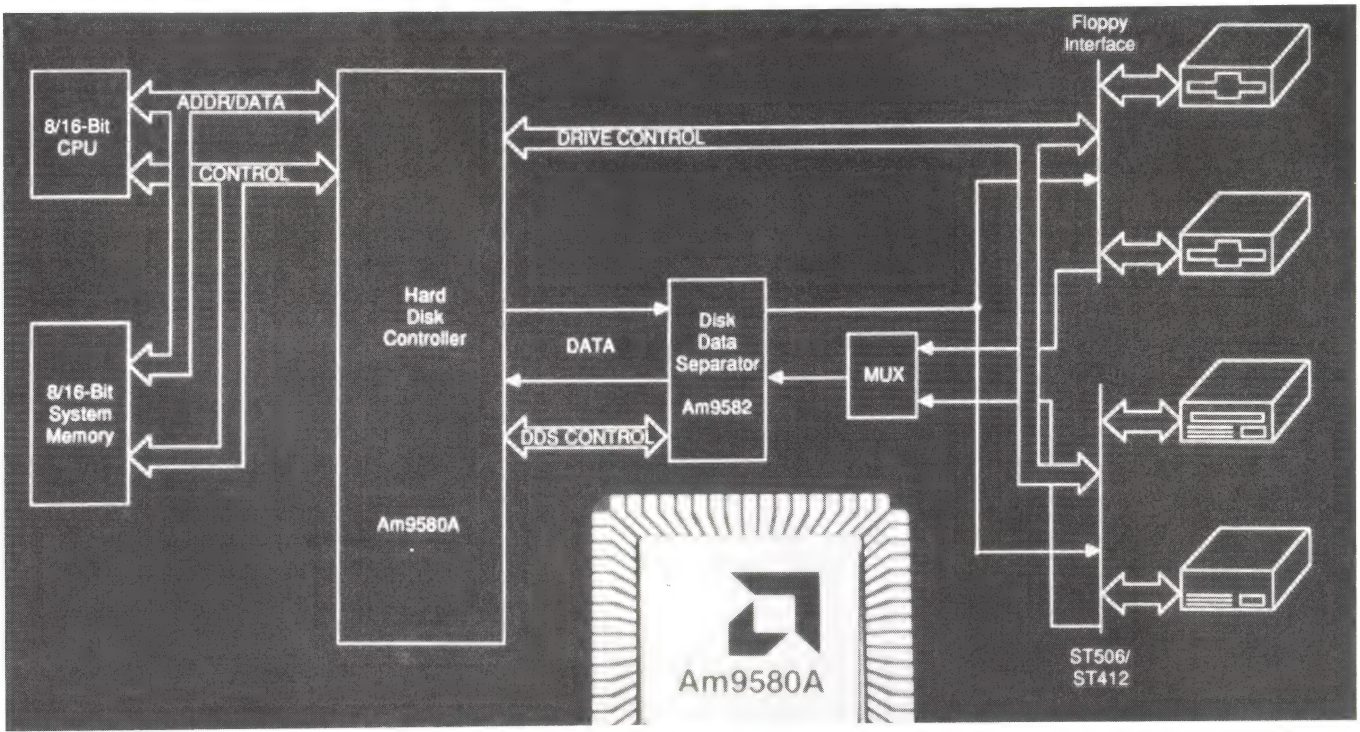
The two sector buffers in the Am9580 provide high throughput rates. While one buffer is communicating with the disk, the other can communicate with the host. This facility allows the IC to accommodate zero-sector interleave, and it reduces file-access time by reducing the number of disk revolutions needed to access data from physically contiguous sectors. The data buffers accommodate programmable sector sizes of 128, 256, or 512 bytes.

The software controls for the Am9580 are built-in disk-I/O primitives called I/O parameter blocks (IOPBs). These data structures reside in memory and specify the commands the controller is to perform. You can link IOPBs together to allow the IC to execute any number of commands sequentially without any host intervention. The linked list also provides seek-overlap operation by searching ahead in the command chain to find active or inactive files.

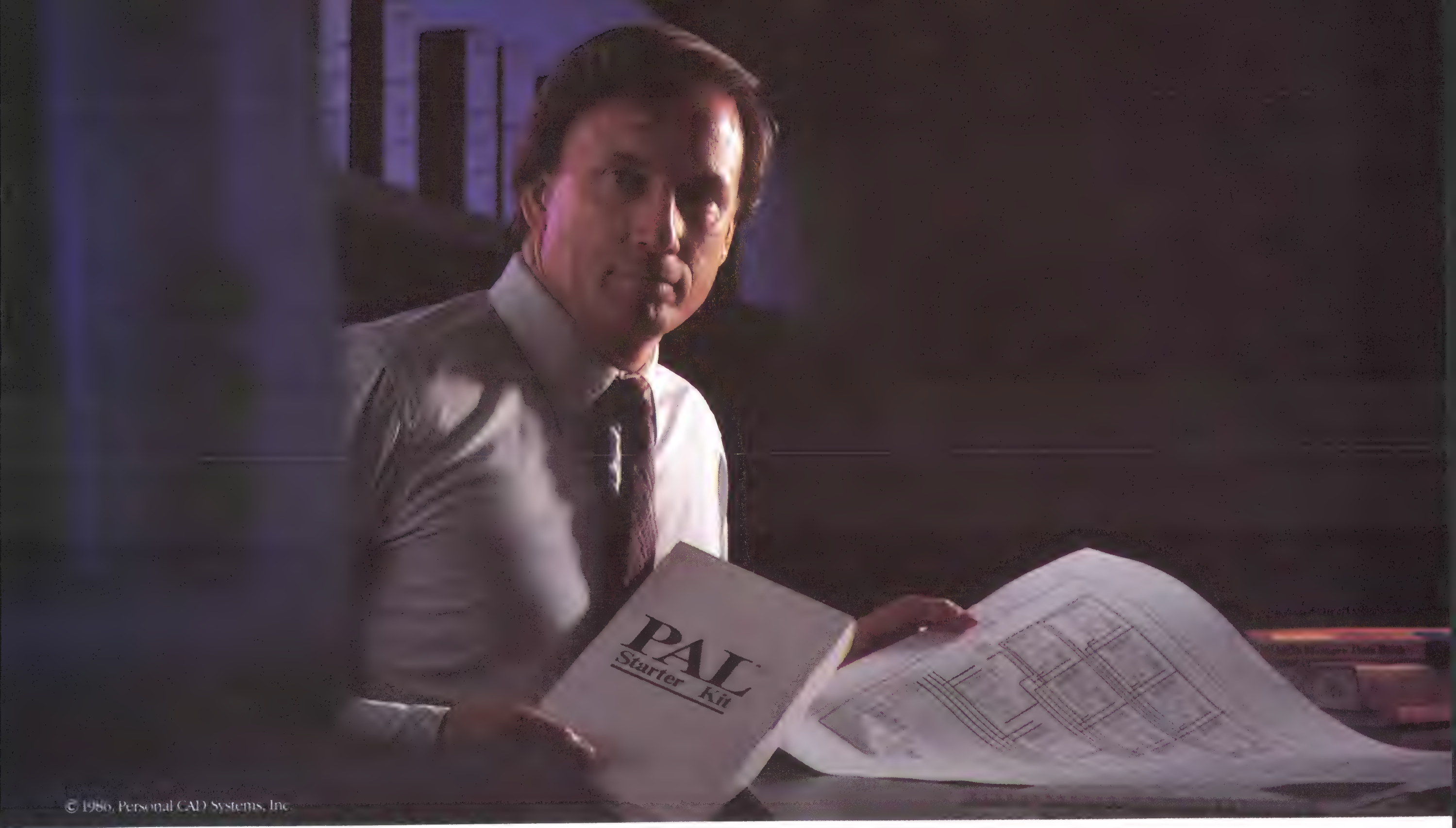
An on-chip DMA controller fetches commands, data, write-status information, and write data from the disks. You can adjust the bus occupancy (burst and dwell time) and the data-word size. The Am9580 works in conjunction with the manufacturer's Am9582 disk-data separator, which is slated for introduction later this year. Packaged in a 68-pad LCC, the Am9580 costs $63 (100).—***Bill Travis***

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 733



Able to replace an entire disk-controller board, *the Am9580 disk-controller IC from Advanced Micro Devices offers three error-detection and correction schemes and accommodates zero-sector interleave. In addition, the chip incorporates a DMA controller, which reduces the need for CPU intervention.*



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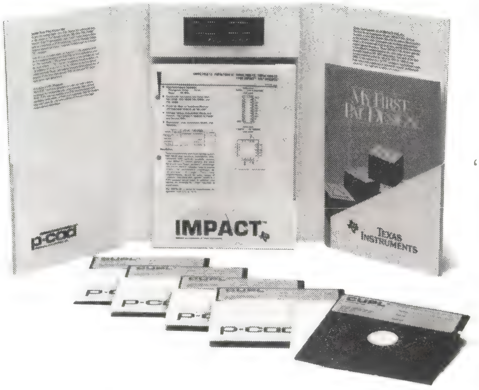

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Development tools let you design graphics applications using the 34010 graphics μP

A set of development tools now supports the TMS34010 Graphics System Processor (see "Graphics ICs," EDN, February 6, 1986, pg 104), which combines general-purpose 32-bit μP features with special graphics-processing hardware. You can control the TMS34010 with programs written in C or assembly code. Included in the development-tool set are an assembler, a C compiler, function libraries, an in-circuit emulator/debugger, and a software-development board.

The assembler package generates common object-file-format section-oriented object code for IBM PCs and compatible computers running MS-DOS 2.11 or higher. (Versions for VAX computers are also available.) The assembler package includes a 34010 simulator that provides a screen-oriented software debugger with breakpoint/trace operation, graphics simulation, instruction execution, input redirection, an environment-save/restore function, and an on-line help utility.

The C compiler for the 34010 supports full Kernighan and Ritchie C with extensions for in-line assembly code and enumerated data types. It has a 3-pass optimizing preprocessor, parser, and code generator that produces 34010 assembly source code. The compiler provides memory management and 64-bit floating-point operation with run-time support.

The graphics/math software library includes graphics primitives, transcendental functions using double-precision floating-point math, matrix operations for 3-D transformation, text generation, view-port support, some basic fonts, and color-palette management. The font library has 19 different font styles, with pixel heights ranging from 7 to 82 pixels, for a total of 106 fonts.

The XDS/22 in-circuit development system provides real-time 34010 emulation. You can use the emulator in a stand-alone mode via a standard terminal or through a host computer with a debugger interface. The XDS/22 also performs full-speed hardware traces and permits multimode single-step/breakpoint operation for generating benchmark specs.

The 34010 assembler package costs $500 for the IBM PC version. The C compiler costs $1000; the graphics/math software library, $10,000; and the font library, $5000. The XDS/22 development system costs $14,995.—***J D Mosley***

Texas Instruments Inc, Semiconductor Group, Box 809066, SC-636, Dallas, TX 75380. Phone (800) 232-3200.

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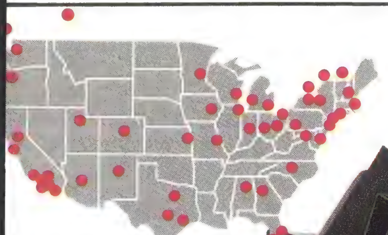

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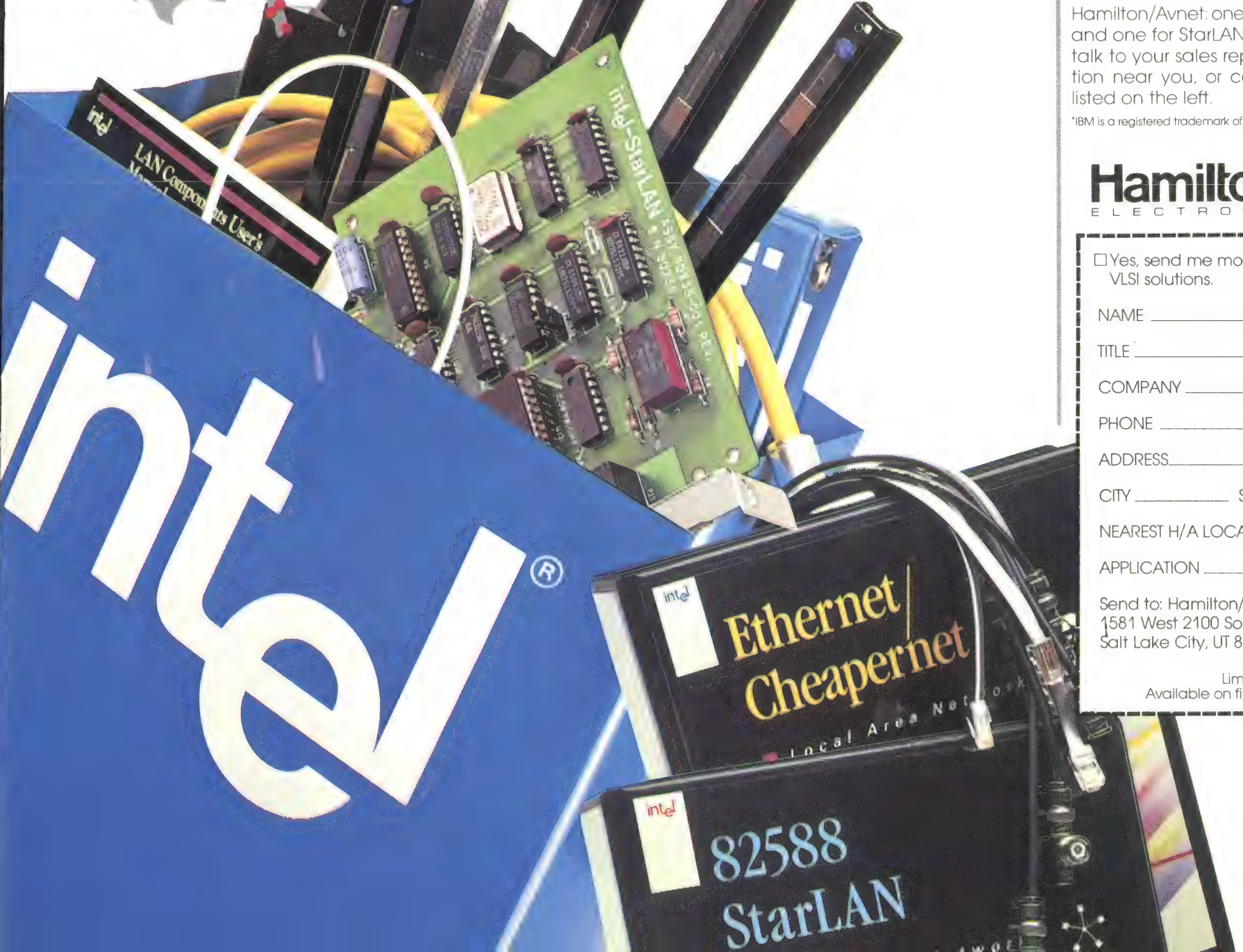

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CIRCLE NO 84

Chip set supports the 16-MHz 80386 µP and offers compatibility with PC/AT

The CS8230 AT/386 chip set is a 7-chip implementation of the support ICs required for a system based on Intel's 16-MHz, zero-wait-state 80386 µP. Compatible with existing PC/XT and PC/AT architectures, the set cuts the total number of support ICs required for an 80386-based PC/AT mother board from 125 to 30 (plus memory), and it shrinks the board size by more than half—to 50 in^2. Furthermore, in anticipation of the introduction of a standard-creating 80386-based machine, the chip set is not limited to support of the PC/AT.

The CS8230 consists of an 82C301 bus controller, 82C302 or 82C312 memory controller (all in CMOS), an 82A303 and -304 address bus interface, an 82A306 control signal buffer (all in advanced low-power Schottky), and two 82B305 data-bus interfaces (in bipolar and CMOS circuitry).

The 82C302 and 82C312 memory controllers support interleaved and cache memory configurations, respectively. Both configurations take advantage of the 80386's pipeline capability to speed memory accesses and to run with zero wait states.

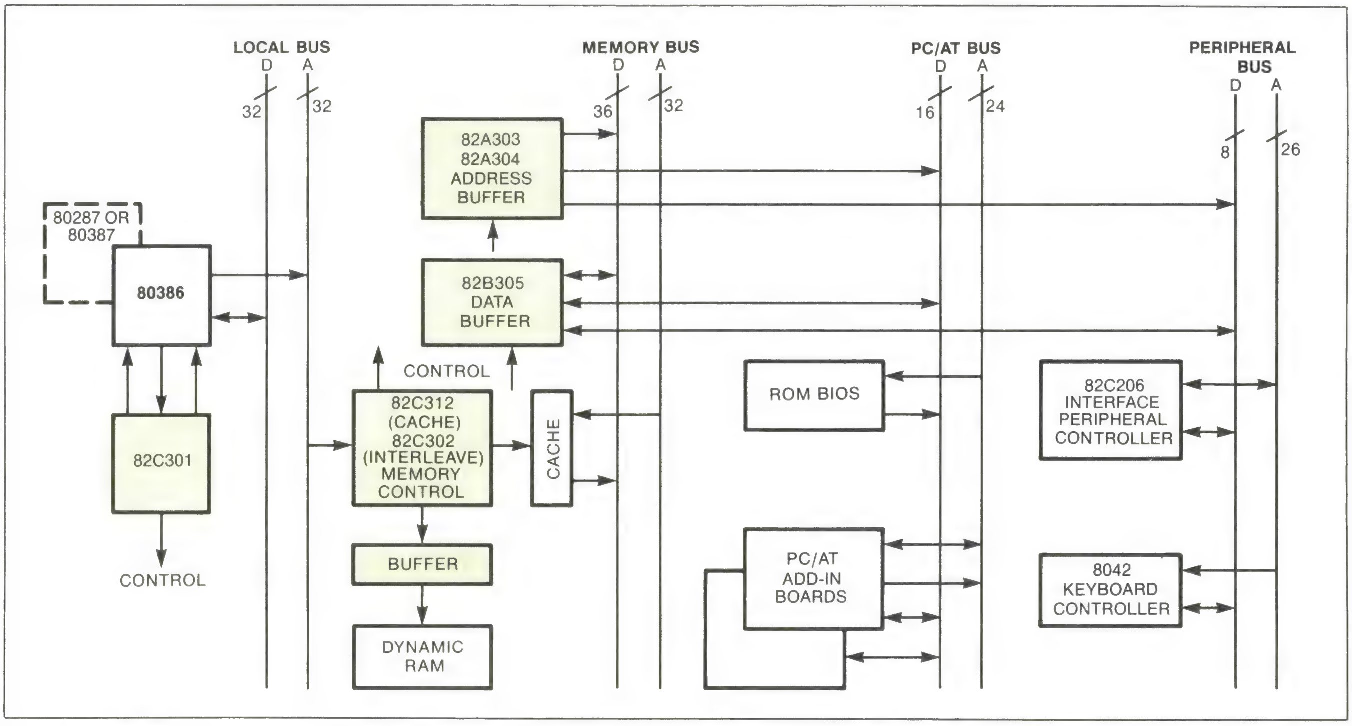
The success rate for anticipating the next instruction in an interleaved configuration is about 70%, and about 90% in a cache configuration. In addition to the cache design's higher performance, it offers an easier path for memory expansion. Moreover, the cache design has no minimum memory size and can hold as much as 64M bytes; the interleaved configuration supports only 1M to 32M bytes. However, the advantages of the cache design are balanced by a price premium for the 82C312 plus the need for 16k bytes of the more expensive static RAM that makes up the cache.

Current add-in boards for the PC/AT are designed for compatibility with an 8-MHz, 1-wait-state clock. To handle these boards, the chip set switches between a 16-MHz clock for internal timing and a lower-frequency clock for system timing.

The CS8230 set is available in sample quantities now; production quantities will be available in the first quarter of 1987 and will cost $130 (5000).—***Margery S Conner***

Chips and Technologies Inc, 521 Cottonwood Dr, Milpitas, CA 95035. Phone (408) 434-0600.

Circle No 731



In this PC/AT-compatible system, *an 82C301 generates control signals for the local, memory, PC/AT, and peripheral buses. The 82A303 and -304 provide the interface between the address buses; two 82B305s provide the interface between the data buses. The 82C302 or -312 implements the interleaved or cache memory options, respectively. Phoenix Software (Norwood, MA) supplies the PC/AT ROM BIOS. Chips and Technologies supplies the 82C206, which is not part of the CS8230 set.*

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CIRCLE NO 85

1086EDN911

High-performance mainframe scopes offer touchscreen control, interactive menus

The 11000 Series mainframe oscilloscopes will eventually replace most of the manufacturer's 7000 Series modular laboratory oscilloscopes. Currently, the 11000 Series comprises two analog mainframes, two digitizing mainframes, five plug-in amplifiers, and three probes.

The mainframes, which have built-in timebases, accept as many as three vertical-amplifier plug-ins. You can control the scopes remotely over built-in IEEE-488 or RS-232C interfaces.

Both the analog and the digitizing mainframes display eight traces, provide extensive on-screen readouts of setup and measurement parameters, and perform built-in signal processing. The scopes use touchscreens and menus in lieu of many of the knobs and switches found on older oscilloscopes (such as the Series 7000 scopes). Further, the 11000 Series scopes perform an automatic calibration—from probe tip to CRT—at the press of a button.

The 500-MHz 11302 and the 400-MHz 11301 analog mainframes have built-in, 500-MHz counter/timers. You can display the counters' input on the scopes' CRTs. Besides making counter/timer measurements, the scopes automatically measure peak-to-peak amplitude, frequency, and duty cycle.

The digitizing mainframes, the 11402 and the 11401, feature 1-GHz and 500-MHz analog (and repetitive digitizing) bandwidths, respectively. Both mainframes have 10-bit vertical resolution and can capture as many as 10k points per waveform. The mainframes can store a total of 100k points.

You can choose as many as six measurements; the digital scopes update them continuously on screen. When the instruments' temperature range is exceeded or the configuration is changed, the scopes' enhanced-accuracy mode warns you that the machines are no longer capable of their highest accuracy.

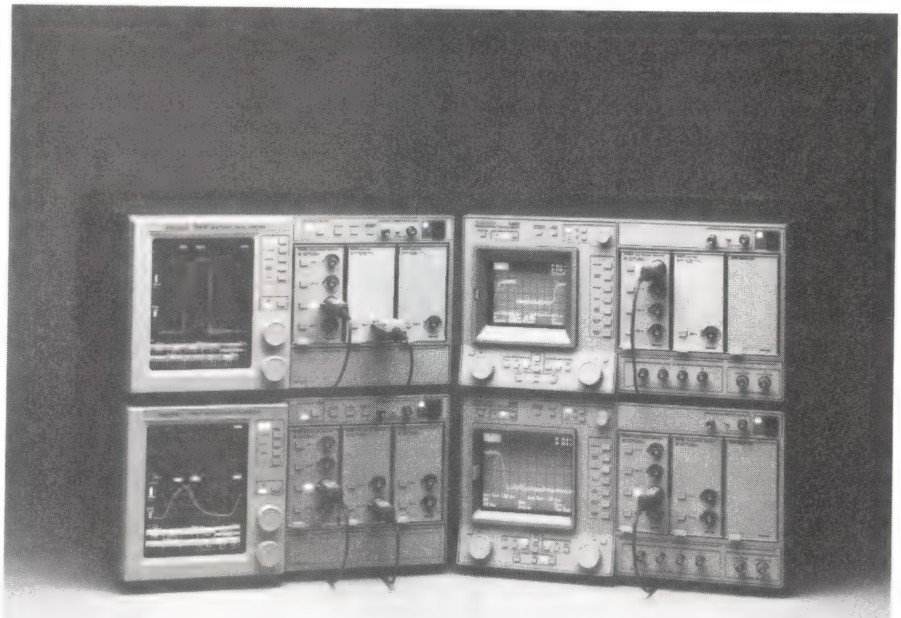
The vertical-amplifier plug-ins comprise the single-channel, 1-GHz 11A71; the dual-channel, 600-MHz 11A52; the dual-channel, 375-MHz 11A32; the 4-channel, 325-MHz 11A34; and the differential-input, 150-MHz 11A33. The plug-ins are all under the control of the mainframe. The only switches on the plug-ins simply turn a given trace on and off.

The plug-ins will accept conventional probes having BNC connectors, as well as three probes designed for the 11000 Series: the 10-MΩ P6134; the P6135 differential probe; and the 450Ω P6231 active probe. Each of the new probes has additional contacts, along with its BNC connector, for identifying the probe, powering active probes, or coupling probe-tip switches to the mainframe.

The 11302 analog mainframe costs $12,950; the 11301 is $8550. The 11402 and 11401 digitizing mainframes cost $15,500 and $13,000, respectively. The 11A71, 11A52, 11A32, and 11A33 plug-ins sell for $2700, $2405, $2025, and $3000, repectively. The probes cost $170 to $500.—***Charles H Small***

Tektronix Inc, Marketing Communications Dept, Box 1700, Beaverton, OR 97077. Phone (800) 547-1512; in OR, (800) 542-1877.

Circle No 735



Four mainframe oscilloscopes*—two analog and two digitizing scopes—replace the forest of knobs and switches found on earlier high-performance, laboratory-grade scopes with touchscreens, menus, and context-dependent controls.*

☐ 6½ digits, ±3,000,000 counts ☐ 100 nV, 1 nA, 100 $\mu\Omega$ sensitivity ☐ 30 ppm DCV accuracy
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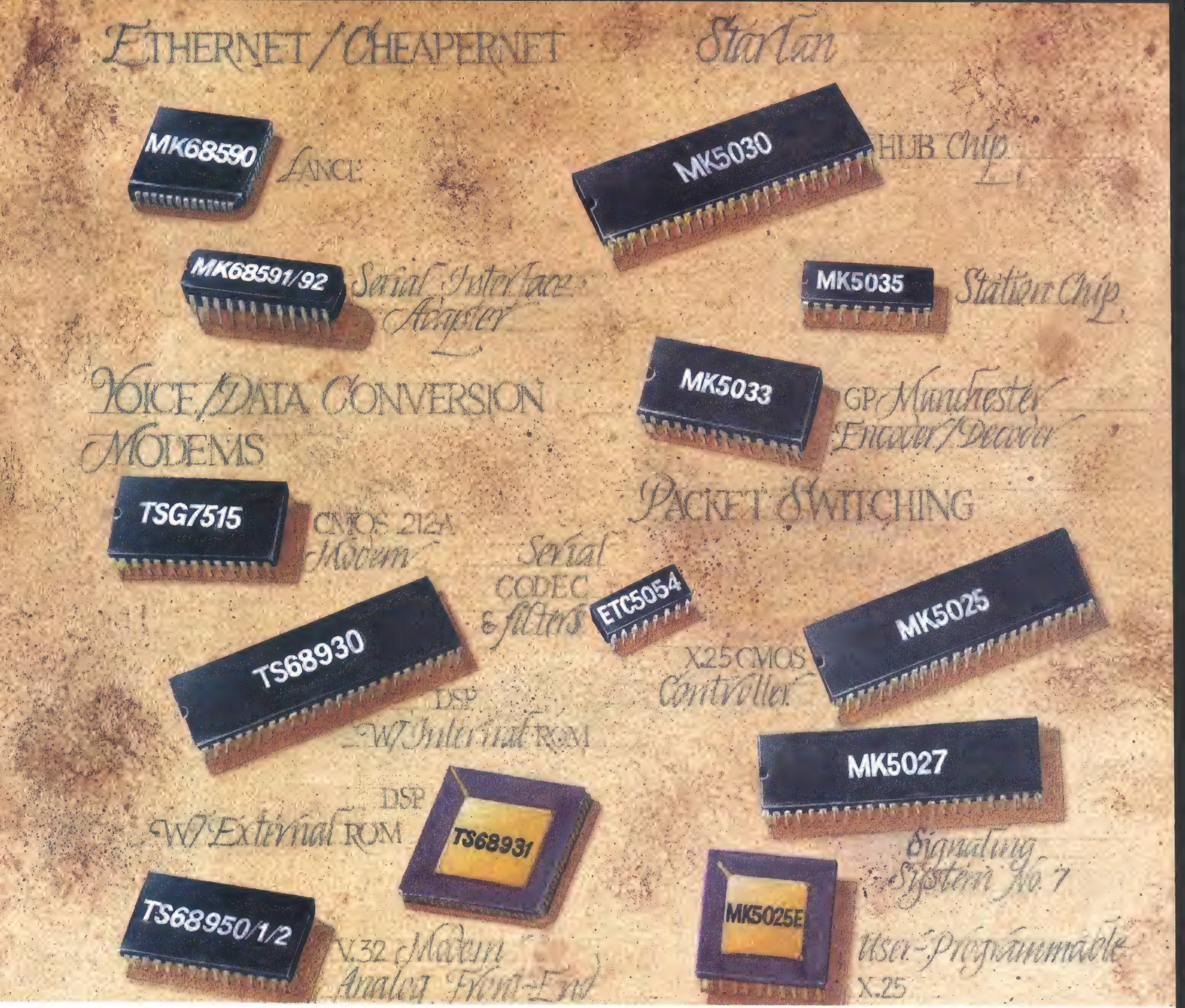
Call or write Keithley for more information.
Product Information Center, Instruments Division, Keithley Instruments, Inc., 28775 Aurora Road, Cleveland, Ohio 44139, (216) 248-0400.

CIRCLE NO 86



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CIRCLE NO 88

Flat-panel terminal sports light-emitting display

If you can't find enough space on your desk for a conventional CRT terminal, consider the flat-panel alternative: The FT-50 features an 8.5×11×2.5-in. display and a 1.5×14×5-in. keyboard. Its total shipping weight is 3.5 lbs.

An average CRT can occupy 140 in^2 of desk space, but the FT-50's display takes up only 25.5 in.^{2} You can order either an electroluminescent (EL) or a gas-plasma version. Both provide 80-character×25-line, 4×8-in. display areas. A 5×7-dot matrix defines characters in a 6×10-dot cell. A double-height/double-width display option generates 40×12-dot characters. The life expectancy for either display is 30,000 hours, which is approximately three times the life expectancy of a CRT.

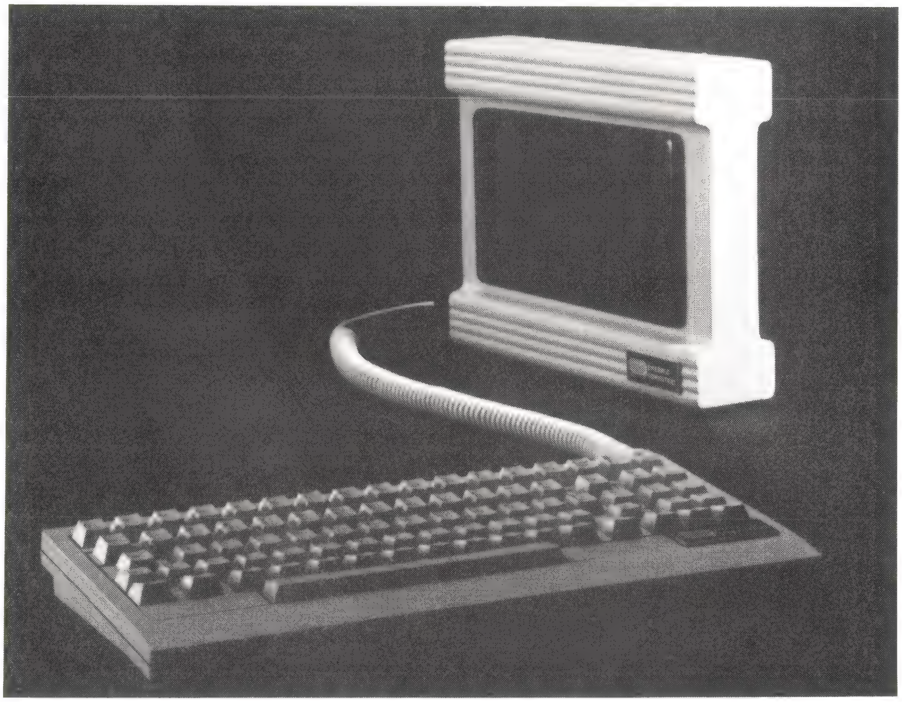
The flat-panel display's video attributes include blink, blank, underline, reverse, and protect; these attributes can be combined for special effects. You can define the cursor as a blinking or nonblinking block or underline. The FT-50 uses 96 ASCII characters, 16 control-code symbols, and 16 graphics characters.

The keyboard attaches to the display via a coiled cable. Its 10 function keys are segregated from the 63-key alphanumeric layout. Cursor and edit keys are included, as are two asynchronous RS-232C ports.

The FT-50 meets ANSI standard 3.64, and it's compatible with IBM, DEC, Televideo, and Wyse terminal protocols. $1295 (100). Delivery, six to eight weeks ARO.—***J D Mosley***

Emerald Computers Inc, 16515 SW 72nd Ave, Portland, OR 97224. Phone (503) 620-6094.

Circle No 728



Featuring a light-emitting flat-panel display, *the solid-state FT50 terminal occupies a fraction of the desk space required by conventional CRT terminals and weighs only 3 lbs.*

Debugger speeds programming for PCs that use EGA cards

For use with Enhanced Graphics Adapter (EGA) programs, the dBUG/EGA assembly-code debugger can set breakpoints and select colors, and it allows you to create custom fonts. It comes with a demonstration program of basic animation techniques.

Traditional debuggers access only .COM or .EXE files to display register and memory contents. To improve on that scheme, dBUG/EGA loads your .LST file and displays the source code (with the current instruction marked) along with the corresponding register and memory contents; consequently, you can identify subroutines and constants by their labels and names. In addition, a program-flow diagram appears in a separate window.

The color command speeds color selection and design by allowing you to experiment with color combinations. To select a color, simply type "Cn" ("n" represents the palette's color-selection number). Without the debugger, changing a color would require you to edit, recompile, and rerun a program before you could see the new color design.

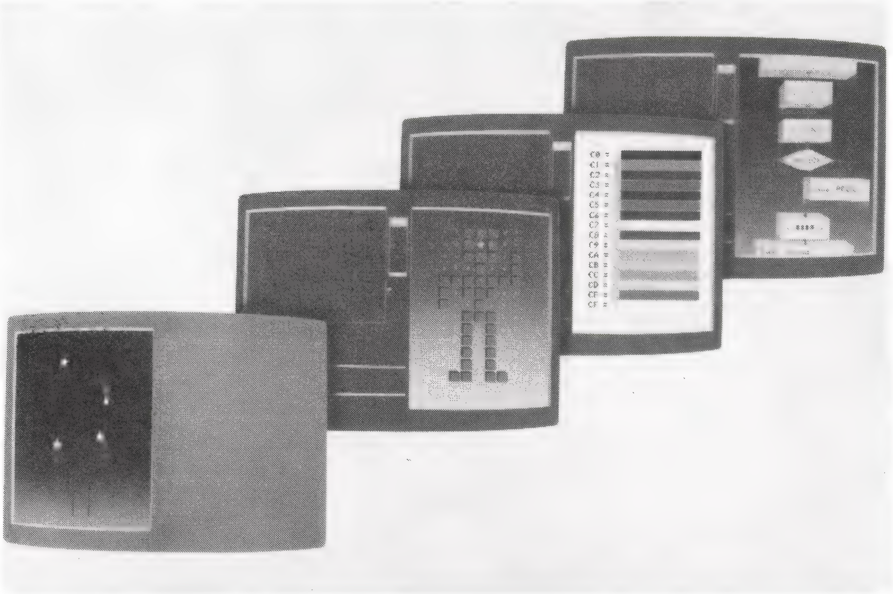
Similarly, you can create and test a new font immediately by using the font-creation command. That command enables you to use the cursor keys to select a pixel within the 8×14-pixel font array; the "=" and "−" keys turn the pixel on or off.

The dBUG/EGA package costs $99 (unprotected) and runs on an IBM PC/XT, PC/AT, or compatible computer with a minimum of 256k bytes of RAM and a 256k-byte EGA or compatible board. The manufacturer also offers EGA utility source code ($99) consisting of the font-creation and -loading code and geometric-pattern-generation routines.

—Margery S Conner

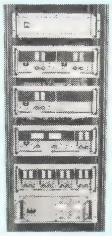
Cybernetic Micro Systems, Box 3000, San Gregorio, CA 94074. Phone (415) 726-3000.

Circle No 727

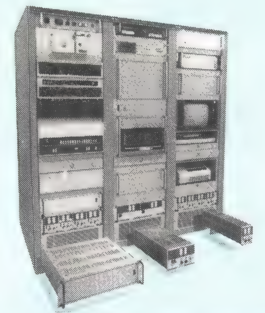


You can debug assembly source code, *create fonts, and design screen colors for Enhanced Graphics Adapter programs with the dBUG/EGA graphics debugger.*

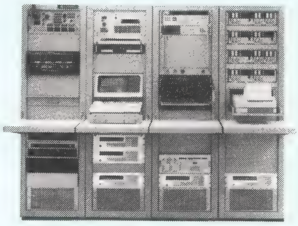
KEPCO POWER MANAGEMENT SYSTEMS™ AT WORK



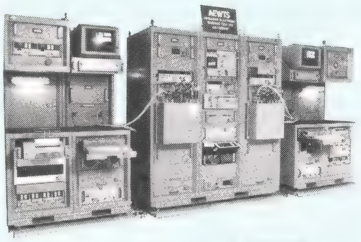
System put together, tested and delivered by Kepco, consisting of one TLD 488-16 controlling five quarter-rack, three half-rack, and one full rack ATE Power Manager.



Grumman CAT™ Test System incorporating one SNR 488-8 controlling 11 ATEs.



Harris Corporation AAN/USM-484 Hybrid Test System with one single channel SN 488-12 controlling 10 ATEs.



Honeywell AEWTS and ETS Tests Sets include one SNR 488-8 to control varying numbers of ATEs.

For 144-page Kepco Applications Handbook and Full Line Catalog, call/write Dept. JLB-12, KEPCO, INC., 131-38 Sanford Avenue, Flushing, NY 11352 USA • (718) 461-7000 TWX #710 582 2631 • FAX: (718) 767-1102.

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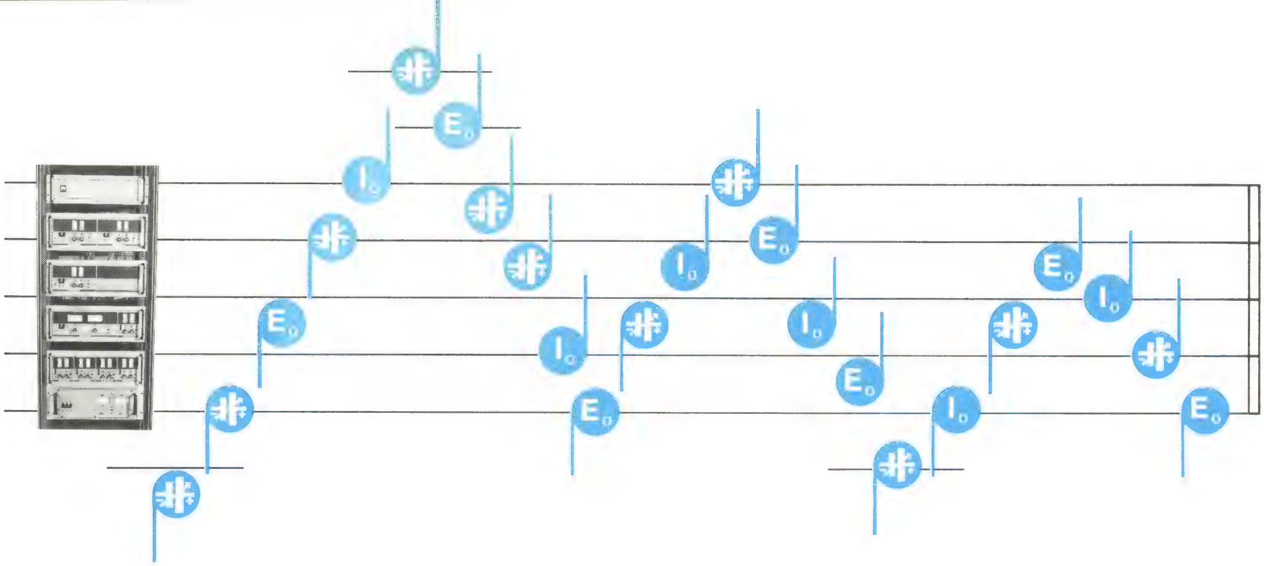
CIRCLE NO 96



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Kepco Power Management Systems™ control voltage to 0.001% and current to 0.005%, and respond to programming step changes in as little as 3 microseconds. They offer the most precise, the most flexible control of power you can buy.

Kepco Power Management Systems consist of components that work perfectly together because they were *designed* to work perfectly together: Kepco Power Managers and Kepco Digital Interfaces.

The Kepco Power Managers are linear programmable power supplies which have been especially designed for programming applications. Their voltage and current can be controlled from zero through their entire range; they can give you maximum rated voltage *and* maximum rated current *simultaneously;* and they can scale a uniform 0-1V or 0-10V control signal into any desired output within their range.

The Kepco Digital Programming Interfaces were created to take full advantage of the Power Managers' precision and speed of response, by allowing them to be controlled by a computer or digital controller. They translate 12-bit digital signals into a 0-1V or 0-10V variable d-c signal, and are guaranteed monotonic to within 1/2 LSB or 0.012%.

There are 12 series of Power Managers, each with its own characteristics.

Series ATE, for example, offers full external control over both voltage and current with automatic crossover; and user selectable *slow mode* for stabilizing voltage, and *fast mode* for stabilizing current and following high speed programming.

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Our TLD Digital Programmer not only passes commands to Power Managers from a computer or digital controller, but also passes responses from the Power Managers back to the computer. It can control up to 16 Power Managers at once.

Our Series SN are stand-alone interfaces, with models available for use with the IEEE bus, or, for fast programming buses using bit-parallel data transfer. Series BIT are cards which plug into the BOP Power Managers.

The Kepco Power Managers are computer-tested and delivered fully zeroed and calibrated, for easy mating with any SN or TLD programmer and quick assembly into an operating system.

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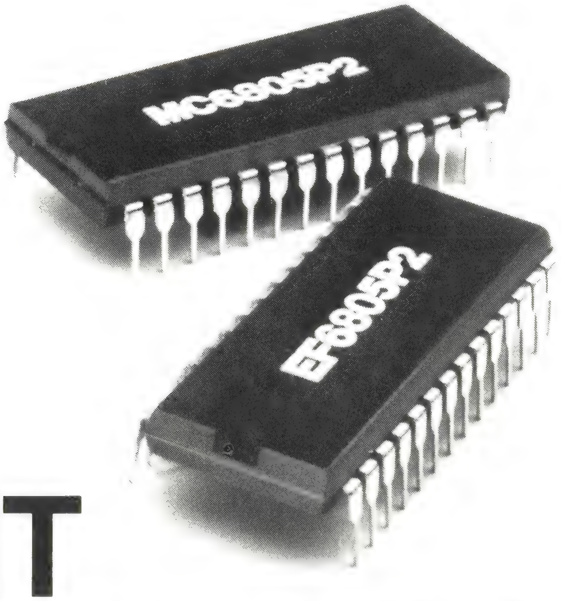
CIRCLE NO 97



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EF6804 FAMILY	8-BIT	MC6804 FAMILY
EF6805 FAMILY	8-BIT	MC6805 FAMILY
MK3870 FAMILY	8-BIT	
EF6801 FAMILY	8-BIT	MC6801 FAMILY
MK68200 FAMILY	16-BIT	TO BE ANNOUNCED

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CIRCLE NO 90

Delta-sigma A/D converter specs 84-dB dynamic range

Using a technique that oversamples input signals for processing by a delta-sigma modulation loop, the CSC5316 A/D converter processes 0- to 4-kHz signals that have an 84-dB dynamic range. This IC is suitable for use in voice-band signal-processing applications such as voice-recognition systems and echo-canceling modems.

(For more information on oversampling and delta-sigma modulation, see the *Digest of Technical Papers* from the 1986 IEEE International Solid State Circuits Conference.)

The chip's modulation loop samples the input and produces a serial 2.048-MHz digital data stream that is decimated by a 384th-order digital filter into a 16-kHz data stream of 16-bit words. Delta-sigma modulation produces a flat group delay for minimum distortion. The CSC5316 specs its ratio of full-scale signal to total harmonic distortion at 72 dB.

This IC features a 3-μm CMOS architecture. It dissipates less than 200 mW. A serial interface with a 4.096-MHz master clock gives the chip codec DSP compatibility. The chip also features an internal 2.048-MHz track/hold amplifier, an internal voltage reference, and a data-conversion speed of 62.5 μsec.

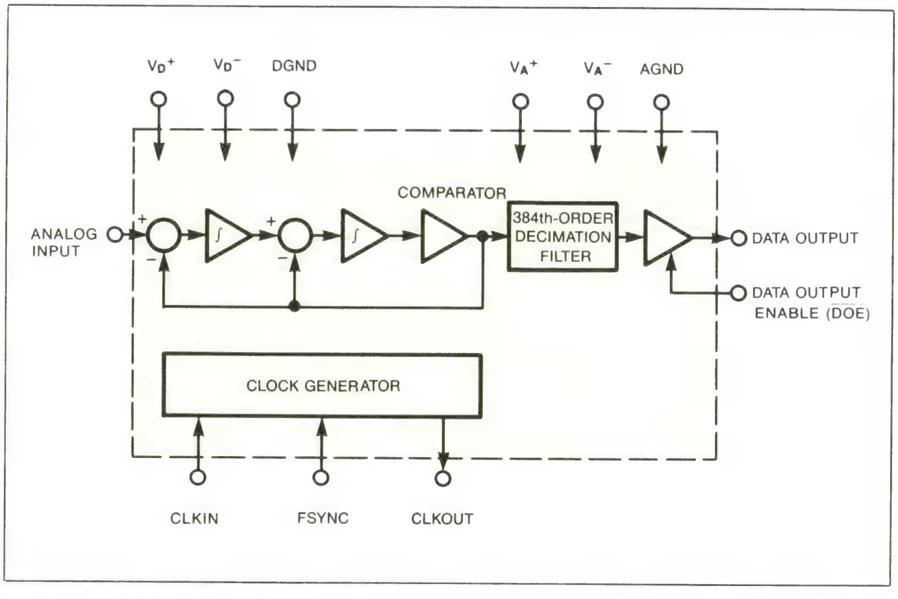
The CSC5316 requires no S/H filter and no reference signal. If your design requires an antialiasing filter, a 2-component RC circuit will suffice. The IC has independent analog and digital power-supply pins to isolate digital noise from the analog circuitry.

Packaged as an 18-pin DIP, the CSC5316 costs $30 (1000). You can also order a ceramic version.

—J D Mosley

Crystal Semiconductor Corp, Box 17847, Austin, TX 78760. Phone (512) 445-7222.

Circle No 726



Offering 84-dB dynamic range, *the CSC5316 uses a delta-sigma modulation technique to reduce distortion and increase resolution in voice-band DSP applications.*

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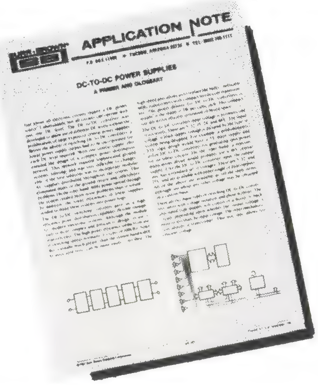

APPLICATION NOTE
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CIRCLE NO 102

Hybrid track/hold amplifier easily drives flash ADCs

The CLC940 high-speed, hybrid-circuit track/hold amplifier makes it easy to drive flash A/D converters. The amplifier's speed parameters make it suitable for driving the fastest available flash devices. For example, its hold-to-track acquisition time is 10 nsec to a 1% error band, 16 nsec to a 0.1% band. Track-to-hold settling time to within 1 mV of final value is 12 nsec. The aperture jitter, an important determining factor in a T/H device's speed, is 1 psec. Finally, the hybrid's small-signal bandwidth and slew rate are 150 MHz and 470V/μsec.

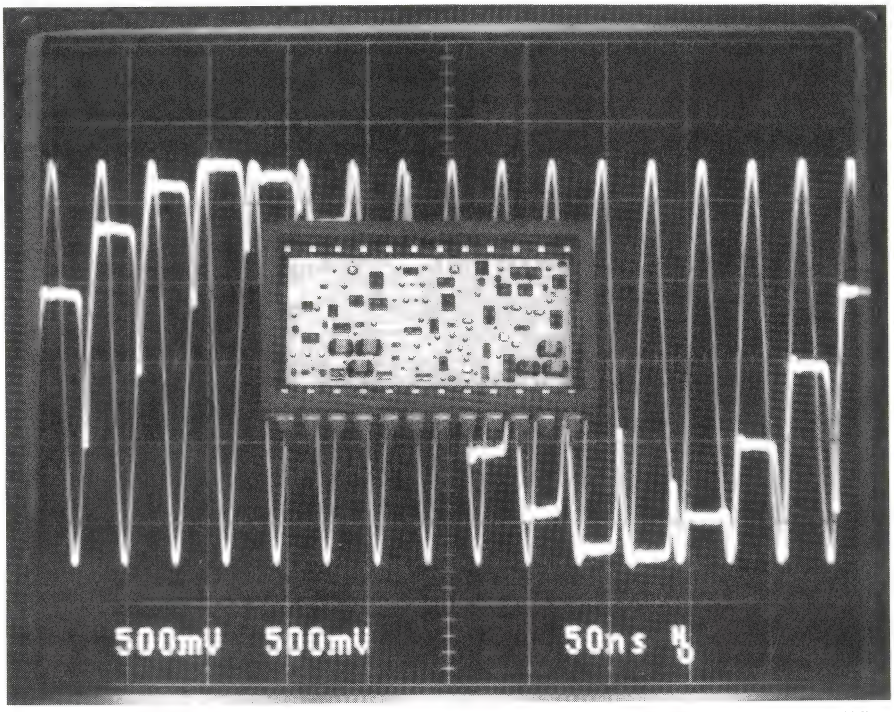
Other specs include 0.02% gain nonlinearity, 20-ppm/°C gain drift, 74-dB feedthrough rejection, and −65-dBc harmonic distortion. Pedestal offset is 2 mV, and (important for linearity) the sensitivity of the pedestal to the input voltage is just 0.03 mV/V. The device's onboard hold capacitor provides a droop rate of 20 μV/μsec.

Capable of accepting either ECL or TTL T/H control signals, the CLC940 operates from ±15V supplies and dissipates 1.6W. Its nominal input-voltage limits are ±2.2V, but it can accommodate a ±2.5V swing at the input. Packaged in a 24-pin DIP, the T/H amplifier is available in both a commercial (−25 to +85°C) and a high-reliability military (−55 to +125°C) version. The two versions cost $196 and $397 (100), respectively. A high-frequency evaluation board costs $10.

—Bill Travis

Comlinear Corp, 4800 Wheaton Dr, Fort Collins, CO 80525. Phone (303) 226-0500.

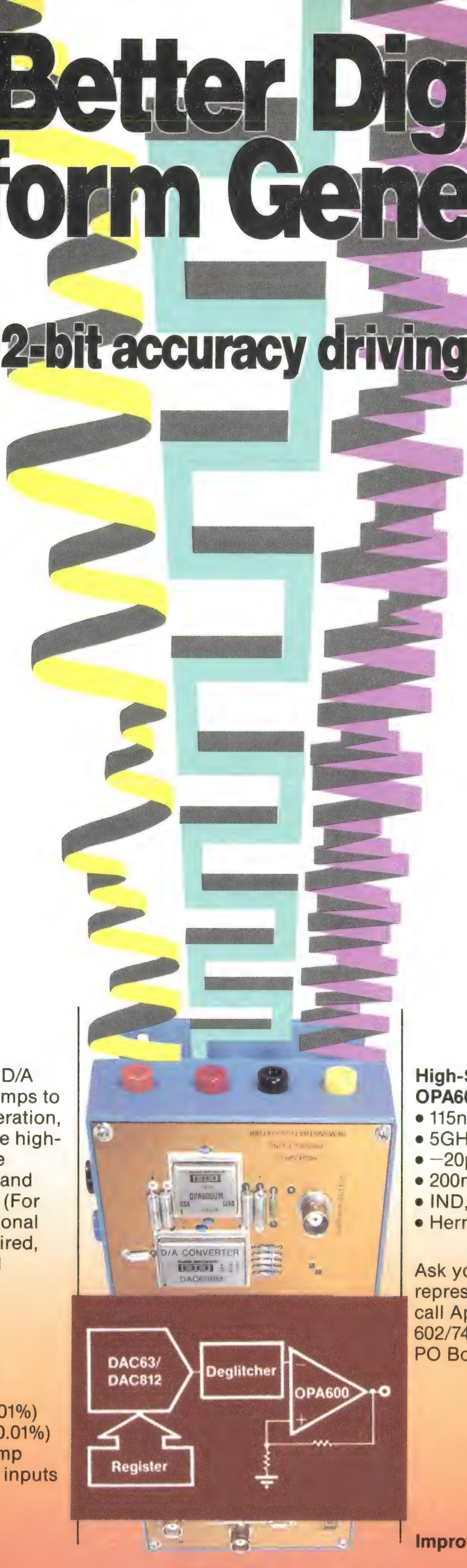
Circle No 734



Driving a flash A/D converter is an easy task *when you use the CLC940 track/hold amplifier. The device has speed and accuracy specs that make it suitable for the fastest available flash units.*

Build Better Digital Waveform Generators

Up to 5MHz, 12-bit accuracy driving into 50Ω load



Use our fast DAC63 and DAC812 D/A converters and new OPA600 op amps to make outstanding waveform generation, test, and line driver circuits. These high-performance parts give you a rare combination of speed, accuracy, and power at very competitive prices. (For high frequency waveforms, additional deglitching circuitry may be required, such as our SHC600 sample/hold amplifier.)

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CIRCLE NO 103

AVAILABLE NOW. GOING FAST.

The fastest family of CMOS 4Kx4 static RAMs ever available. Now available from Thomson Components-Mostek Corporation.

Since we used the same basic design to create the entire MK41H68 family, our six new fast SRAMs share certain features. Like access times of 20ns. And industry-standard 20- or 22-pin JEDEC packaging. But that's where the similarities end. Because each of the six devices offers different features – Chip Enable power down, fast 10ns chip select access or output enable control – you can choose the best solution for your application.

Our fast static RAM family includes the first 5-volt 4Kx4s designed to operate at 20ns. The MK41L68 Series is also the industry's first LSI circuit specifically designed for the new scaled MOS 3.3-volt LV-TTL JEDEC standard. And they're available with access times of 25ns or 35ns. Either way, they're the fastest 4Kx4 CMOS RAMs available anywhere.

A state-of-the-art sub micron double level metal CMOS process and a unique 6-transistor memory cell allows our new SRAMs to operate at high speeds yet maintain low operating and standby power requirements.

Best of all, our new 4Kx4s are available right now. In quantity. From any of our 112 distributor locations nationwide. And it doesn't end there. In the future, we'll be introducing an even wider range of fast static devices, with MIL-883 Rev C followed by JAN qualified versions.

But don't wait too long to find out more. Because with speeds like these, they're going fast. For more information, call 214/466-6265 or contact your nearest local sales office.

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CIRCLE NO 91

Software-controlled CMOS IC replaces manual DIP switches

You can now use software commands to define computer parameters that are ordinarily selected by hand with onboard DIP switches. A 14-pin, battery-backed CMOS IC called the Eliminator (DS1290) replaces eight mechanical DIP-switch settings; a 22-pin version (DS1292) replaces 16 mechanical settings.

These ICs let you design pc boards that end users can customize without extensive technical support, because you can embed the available options—like printer format, modem baud rate, and memory size—in menu-driven software. Software control lets end users set and reset switches without dismantling computers or peripherals.

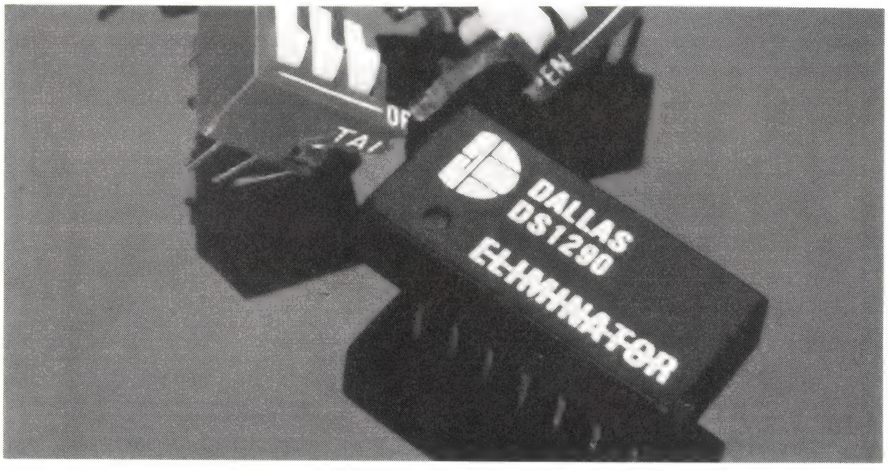
Incorporating an Eliminator on a board requires a DS1206 Phantom interface, a 14-pin IC that plugs into your board under a standard byte-wide RAM. The DS1206 acts as a 3-wire serial port that can control as many as 10 Eliminators. The interface operation is transparent to memory: Software-generated memory cycles activate the serial port and transfer data to a targeted Eliminator. The DS1206 comes on line to set or verify the switch settings only upon a user's request.

Unlike mechanical DIP switches, the Eliminator doesn't need onboard pullup resistors to reach logic levels. Its switches change simultaneously upon software command without interfering with system operations. Once programmed, the Eliminator's switch settings will maintain their high- or low-level outputs. You can cascade DS1290 chips to provide additional switches and modular expansion.

For an introduction to the Eliminator, the manufacturer offers an evaluation kit that includes a DS1290, a DS1292, a DS1206, and an IBM-compatible demonstration disk. The kit also includes samples of other related products, such as a DS1250 interface chip that plugs into a 28-pin byte-wide socket, a DS1201 Configurator chip, and a DS1201 Electronic Tag. The evaluation kit costs $60. DS1290, $1.49; DS1292, $1.99; DS1206, $0.99 (10,000).—***J D Mosley***

Dallas Semiconductor Corp, 4350 Beltwood Parkway, Dallas, TX 75244. Phone (214) 450-0400.

Circle No 729



Offering software control of as many as 16 switch settings, *the solid-state, battery-backed Eliminator lets end users customize pc boards without dismantling their systems.*

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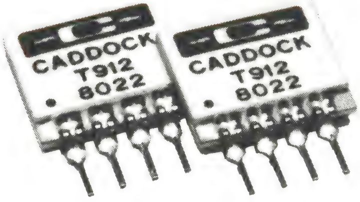
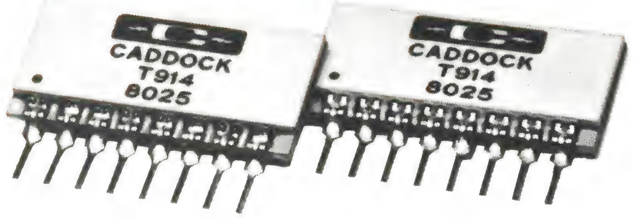
CIRCLE NO 92

Type T912 / T914 Ultra-Precision Resistor Networks from CADDOCK provide Ratio TCs to 2 PPM/°C and Ratio Tolerances to ±0.01% for precision analog designs.



Type T912 Ultra-Precision Resistor Network 'Pairs'



Type T914 Ultra-Precision Resistor Network 'Quads'

Type T912 / T914 Ultra-Precision Resistor Networks are constructed with Caddock's Tetrinox™ resistance films to achieve all of these high performance characteristics:

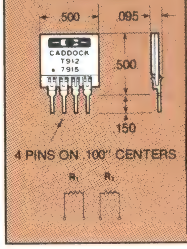
- **Absolute Tolerance:** 0.1% for all resistors.
- **Ratio Tolerances:** From ±0.1% to ±0.01%.
- **Ratio Temperature Coefficients:** From 10 PPM/°C to 2 PPM/°C.
- **Absolute Temperature Coefficient:** ±25 PPM/°C from 0°C to +70°C, referenced to +25°C.
- **Ratio Stability of Resistance at Full Load for 2000 Hours:** Within ±0.01%.
- **Shelf Life Stability of Ratio for Six Months:** Within ±0.005%.

This exceptional combination of performance specifications – and the compact, plug-in configuration of the Type T912/T914 precision resistor 'pairs' and 'quads' – provide the single-package matched resistor characteristics and stability required by high-accuracy analog circuits, including –

- **Precision analog amplifiers.**
- **Voltage reference circuits.**
- **Instrumentation bridge circuits.**
- **Voltage and current comparison circuits.**

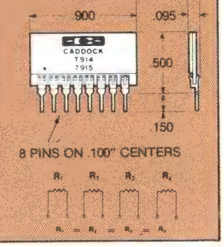
Type T912

Ratios Available: 1:1, 9:1, 10:1 and Custom.



Type T914

Ratios Available: 1:1 and Custom.



Standard models of Type T912 / T914 precision resistor 'pairs' and 'quads' include 14 off-the-shelf resistor values with a wide choice of Ratio Tolerances, Ratio TCs and Resistance Ratios:

This standard part number provides a selection of over 500 in-production models of Type T912/T914 precision resistor 'pairs' and 'quads':

T912 - A 1K - 010 - 10

Model Number:

Ratio Code Letter:

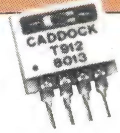
A – T912 with $R_2 = 10R_1$
(Example: 1K – 10K)
B – T912 with $R_2 = 9R_1$
(Example: 1K – 9K)
No Letter – T912 with $R_2 = R_1$
No Letter – T914 with $R_1 = R_2 = R_3 = R_4$

Ratio Temperature Track: (0°C to +70°C)
-10 = 10PPM/°C
-05 = 5PPM/°C
-02 = 2PPM/°C

Ratio Tolerance:
-100 = 0.1%
-020 = 0.02%
-050 = 0.05%
-010 = 0.01%

Standard Resistance Values (R_1):

1K	10K	40K	200K	500K
2K	20K	50K	250K	1 Meg.
5K	25K	100K	400K	

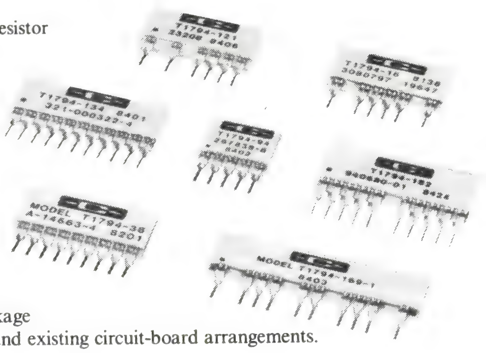


As an example of the price/performance advantages of this advanced resistor technology, the Model T912-A1K-010-10 shown here provides a 1K-10K resistor 'pair' with a ratio tolerance of ±0.01% and a ratio temperature coefficient of 10 PPM/°C at a 1000-lot unit price under $2.66. The same resistor 'pair' with a ratio tolerance of ±0.1% delivers at a 1000-lot unit price under $1.52!

Type T1794 Custom Precision Resistor Networks meet special circuit and packaging requirements:

The Type T1794 custom precision resistor networks provide a unique range of flexibility:

- From 2 to 15 resistors per assembly.
- Absolute tolerances from 1.0% to 0.05%.
- Custom voltage and power ratings.
- Resistance values from 500 ohms to 10 Megohms
- Absolute TC from 50 PPM/°C to 25 PPM/°C.
- Ratio TC from 50 PPM/°C to 5 PPM/°C.
- Variations in pin configurations and package size as required to meet performance and existing circuit-board arrangements.



Caddock's advanced film resistor technology is the source of these outstanding advantages—advantages that are matched by a 20-year record of outstanding 'in-circuit' reliability.

Discover how easily these problem-solving resistors can improve the performance and reliability of your equipment, too. For your copy of the latest edition of the Caddock 24 page General Catalog, and specific technical data on any of the more than 150 models of the 13 standard types of Caddock High Performance Film Resistors and Precision Resistor Networks, just call or write to –

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CADDOCK
HIGH PERFORMANCE FILM RESISTORS

CIRCLE NO 100 • See eem

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The new SSA 100 (Serial Systems Analyzer) is the first and only commercially available pre-processor/simulator that processes data in real-time on up to 8 dual redundant MIL-STD-1553 data buses simultaneously.

Now, not only can MIL-STD-1553 protocol be checked with our SBA 100, but specific data can be viewed, analyzed and reduced in real-time with the new SSA 100.

In addition to monitoring bus activity, dynamic data updates can be simulated in real-time. This means that if a new product is being developed to be implemented on a MIL-STD-1553 bus, full bus simulation can be performed for proper testing of the product.

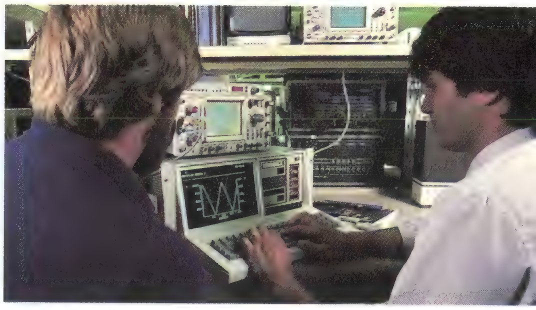
This includes simulation of up to 32 remote terminals (RT's) and multiple bus controller (BC) responses, all in real-time on as many as 8 MIL-STD-1553 dual-redundant buses simultaneously.

The SSA's modular system architecture offers many optional features that make it easier to integrate and test MIL-STD-1553 products. Some options include IRIG time code generation and correlation capability, analog/discrete input and output capability, automatic error and limit checking, as well as a bi-directional DMA channel to a host computer. The DMA allows the SSA 100 to function as a pre-processing element within a system.

As a stand alone, the SSA 100 can pre-filter MIL-STD-1553 data and perform various pre-programmed or user programmable processing algorithms and conversions. This processed data can then be displayed in real-time, by means of tables, charts and graphs for quick look capability.

The SSA can also distribute this processed data through the many available interfaces such as IEEE 488, RS 232, analog/digital outputs, and to mass storage devices via digital tape and disk controllers.

If difficulties with MIL-STD-1553 data analysis and simulation are hindering your progress and causing your schedules to slip, call Loral Instrumentation today.



Systems Integration:
The SSA 100 can simulate expensive or non-existent hardware and software.

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The SSA 100 substantially reduces the time required to write real-time software for the host processor.

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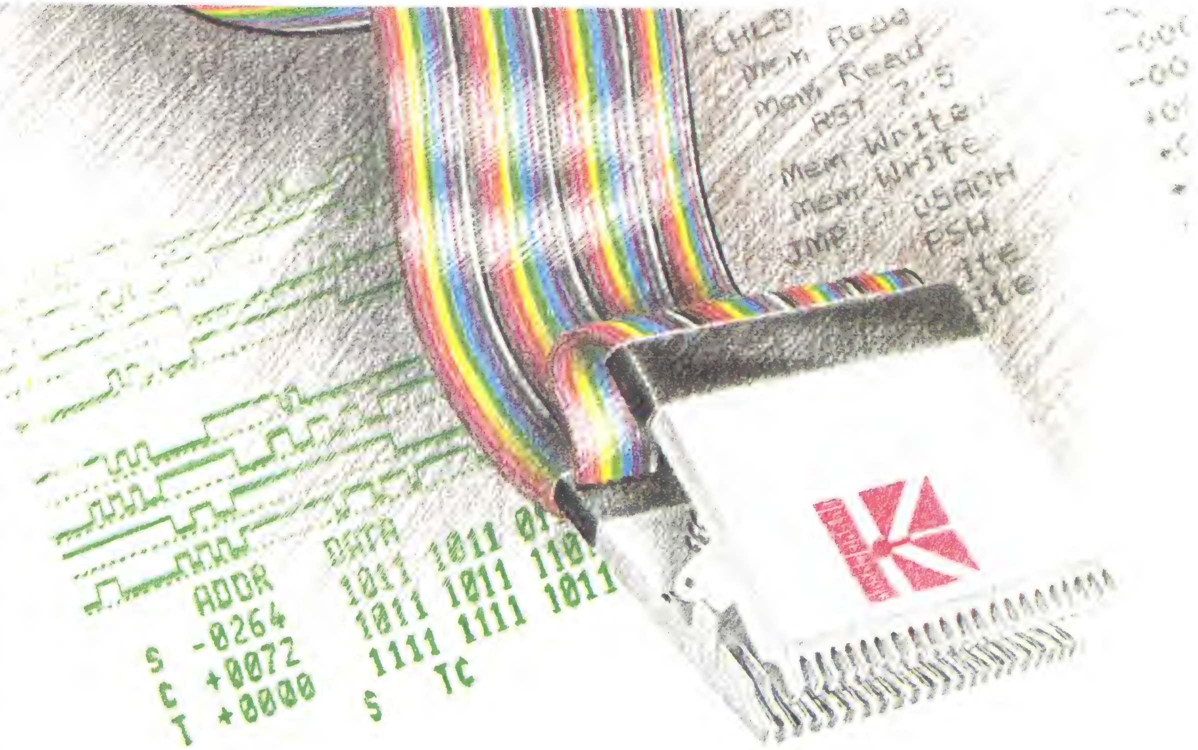
CIRCLE NO 145

INSTRUMENTATION



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CIRCLE NO 99

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CIRCLE NO 104

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READERS' CHOICE

Of all the products covered in EDN's **August 7, 1986,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **August 7, 1986,** issue.

INK-JET PRINTER ▶

The Chromajet 4000 ink-jet printer provides a palette of 1000 distinct color shades for images with resolution approaching 300 dots/in. (pg 222).
Polaroid Corp.
Circle No 606

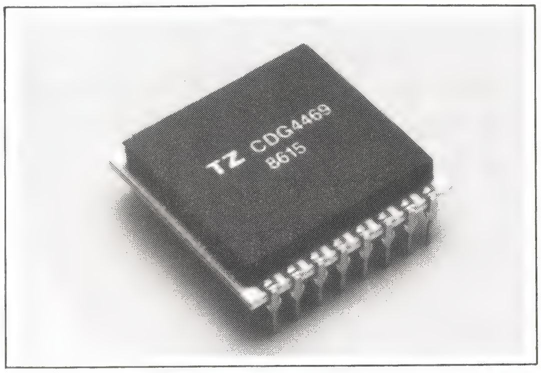
6870X EMULATOR

The PEM-05 is an emulator/programmer for the 68705 single-chip μP family (pg 238).
Mojave Cyber Research.
Circle No 607

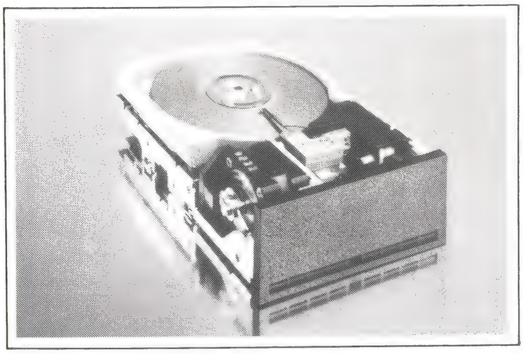
FILTER DESIGN

RF Notes No 3 Volume 2 is a program that solves RF design problems. It designs lowpass, highpass, and bandpass Bessel-response filters (to the 7th order) (pg 221).
Etron RF Enterprises.
Circle No 605

▼ATTENUATOR IC

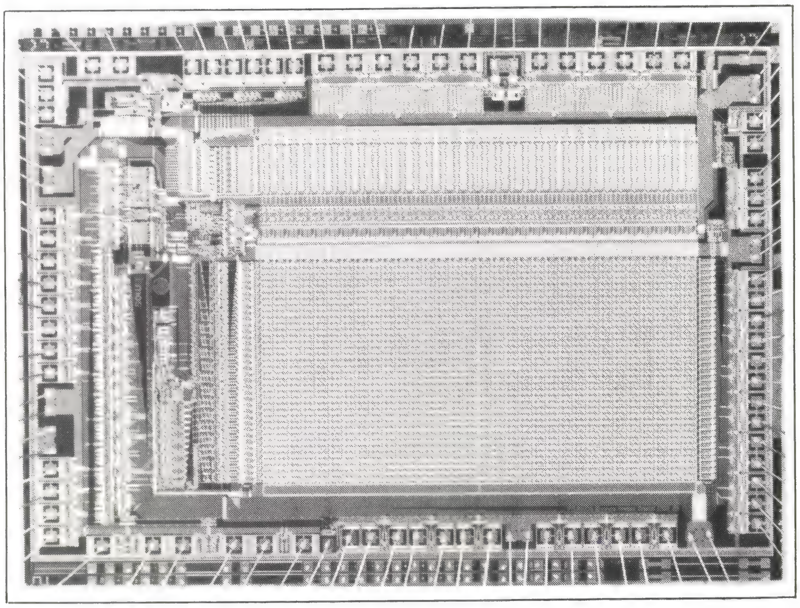


The CDG4469 hybrid attenuator IC uses CMOS logic and level-translation circuitry with lateral DMOS switches to control a ladder network of resistors (pg 117).
Topaz Semiconductor.
Circle No 601



▲ 3½-IN. DISK DRIVE

The 8425S 3½-in. Winchester disk drive incorporates a SCSI controller and provides a capacity of 21.3M bytes (formatted) (pg 124).
Miniscribe.
Circle No 604



▲DSP IC

The IMS-A100 cascadable signal-processor IC integrates 32 multiplier/accumulator stages on a single chip (pg 119).

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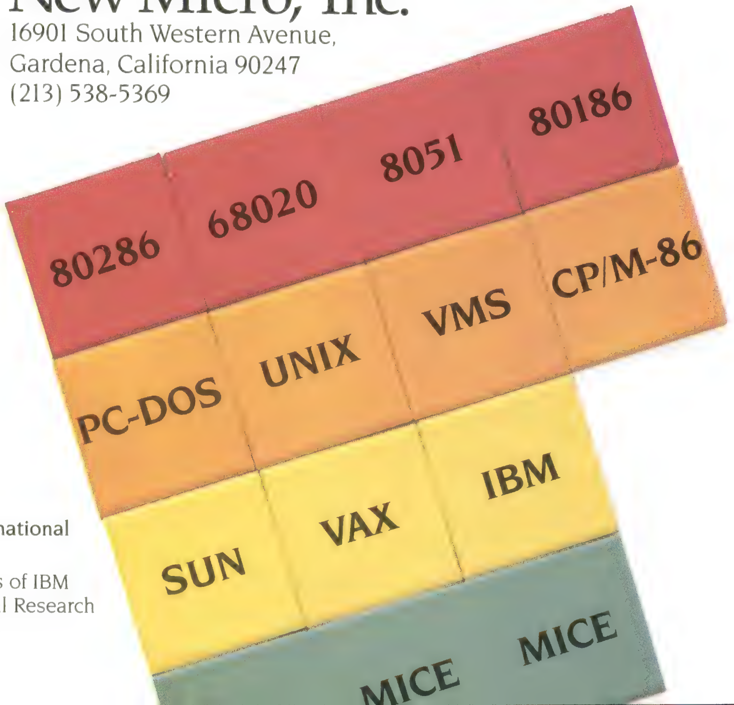

*New Micro, Inc. is the exclusive U.S. distributor for Microtek International in-circuit emulators.

NOTE: PC-DOS, MS-DOS, VAX/VMS, UNIX, CP/M-86 are trademarks of IBM Corporation, Microsoft Corp., Digital Equipment Corp., AT&T, Digital Research Inc., respectively.

CIRCLE NO 105

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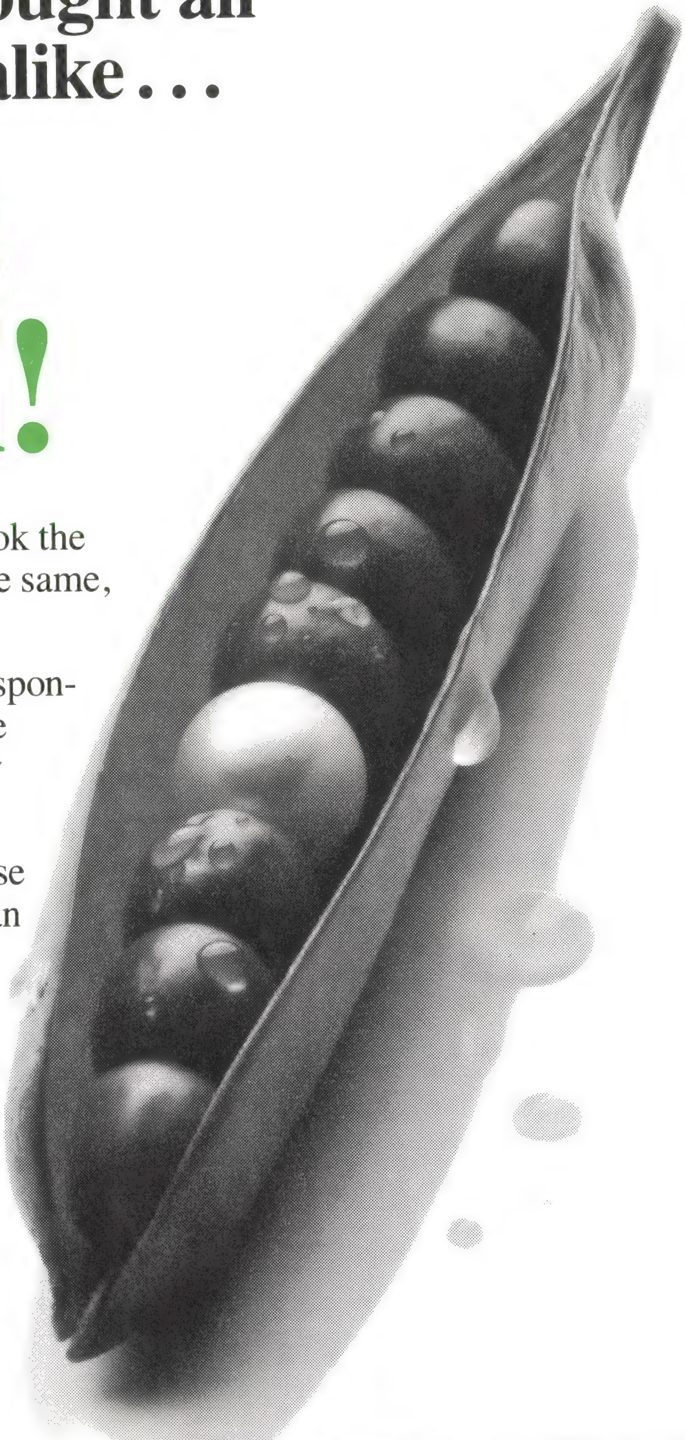

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CIRCLE NO 106

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NEW MIL SPEC SCANNER

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GENERAL SCANNING ANNOUNCES A MAJOR NEW GALVANOMETER!

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THE NEW G4 SCANNER

General Scanning proudly announces the fastest galvanometer ever made for moving large mirrors. The new G4 galvanometer scanner can vector a 1″ × .75″ mirror in 2.5 msec. In addition, this amazing scanner is faster and gives you the best trade-off between speed and angular excursion of any galvo we've ever made.

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The new G4 has zero null drift and less gain drift for increased thermal stability. The superior specifications are possible because of a revolutionary new design and special lightweight mirrors.

CONFORMS TO MILITARY SPECIFICATIONS

Best of all, our first release in the G4 series is built to full military specifications. This product, the G400DM, has a new package design for easy installation while still conforming to the rigorous specifications of MIL-STD-454, MIL-STD-810, and MIL-I-45208.

MORE INFORMATION

For complete information on this exciting new product just send in the attached reply card or call us at (617) 924-1010. A limited number of G400DM's are available on trial order to qualified military programs. Please indicate your interest on the reply card.

GS GENERAL SCANNING INC.

500 Arsenal Street Watertown, MA 02272 Tel: 617/924-1010

CIRCLE NO 108

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average weeks	Last month's average weeks
TRANSFORMERS								
Toroidal	10	20	35	30	5	0	9.3	10.0
Pot-Core	0	28	39	28	5	0	9.6	9.4
Laminate (power)	20	25	40	10	5	0	6.6	8.3
CONNECTORS								
Military panel	0	10	50	20	10	10	13.1	10.6
Flat/Cable	22	37	33	8	0	0	4.6	5.6
Multipin circular	0	7	67	20	6	0	10.4	10.8
PC	20	30	35	15	0	0	5.8	7.9
RF/Coaxial	8	46	31	15	0	0	5.9	7.2
Socket	21	33	33	13	0	0	5.3	7.8
Terminal blocks	17	44	35	24	0	0	4.4	4.9
Edge card	14	19	52	10	5	0	7.3	6.3
Subminiature	13	37	38	6	6	0	6.4	8.4
Rack & panel	8	34	33	25	0	0	7.3	8.2
Power	7	53	27	7	6	0	6.0	7.1
PRINTED CIRCUIT BOARDS								
Single-sided	0	53	47	0	0	0	4.8	5.0
Double-sided	0	36	64	0	0	0	5.8	5.7
Multilayer	0	19	57	24	0	0	8.8	8.9
Prototype	3	81	16	0	0	0	2.9	3.6
RESISTORS								
Carbon film	39	33	20	8	0	0	3.6	3.8
Carbon composition	38	21	31	10	0	0	4.6	7.1
Metal film	21	49	24	6	0	0	3.9	5.9
Metal oxide	20	45	25	10	0	0	4.5	6.6
Wirewound	16	28	40	16	0	0	6.3	6.1
Potentiometers	14	27	43	16	0	0	6.6	7.9
Networks	18	25	32	21	0	4	7.6	7.5
FUSES	33	37	22	8	0	0	3.7	3.6
SWITCHES								
Pushbutton	14	43	32	11	0	0	5.1	5.1
Rotary	4	31	52	13	0	0	6.9	7.2
Rocker	17	28	44	11	0	0	5.9	7.3
Thumbwheel	7	14	57	22	0	0	8.3	11.3
Snap action	24	35	29	12	0	0	4.9	7.4
Momentary	11	50	33	6	0	0	4.6	6.9
Dual in-line	15	39	31	15	0	0	5.7	8.0
WIRE AND CABLE								
Coaxial	39	35	26	0	0	0	2.8	3.9
Flat ribbon	39	29	28	0	4	0	3.8	4.5
Multiconductor	32	41	23	0	4	0	3.8	5.1
Hookup	53	30	17	0	0	0	1.9	2.5
Wire wrap	40	35	20	5	0	0	3.1	3.9
Power cords	18	46	36	0	0	0	3.8	4.2
Other	30	10	30	30	0	0	7.4	8.3
POWER SUPPLIES								
Switching	0	31	35	30	4	0	9.4	9.3
Linear	5	33	38	19	5	0	8.0	9.1
CIRCUIT BREAKERS	13	39	26	18	4	0	6.8	9.3
HEAT SINKS	28	32	24	16	0	0	5.1	7.3

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average weeks	Last month's average weeks
RELAYS								
General purpose	22	26	37	11	4	0	6.2	6.5
PC board	17	33	29	17	4	0	6.8	7.7
Dry reed	10	40	20	20	10	0	8.2	10.5
Mercury	0	30	40	20	0	10	10.1	13.5
Solid state	13	25	31	25	0	6	8.9	8.9
DISCRETE SEMICONDUCTORS								
Diode	15	53	25	5	2	0	4.5	5.4
Zener	18	43	21	18	0	0	5.5	5.2
Thyristor	20	30	25	20	5	0	7.1	7.1
Small signal transistor	21	31	28	17	0	3	6.7	7.3
FET, MOS	5	30	40	20	0	5	8.6	7.7
Power, bipolar	5	43	33	14	0	5	7.3	8.1
INTEGRATED CIRCUITS, DIGITAL								
CMOS	11	33	28	25	3	0	7.6	7.5
TTL	14	24	41	17	4	0	7.5	8.1
LS	12	26	38	21	3	0	7.7	8.5
INTEGRATED CIRCUITS, LINEAR								
Communication/circuit	15	20	45	15	5	0	7.7	10.0
OP amplifier	17	20	27	30	3	3	9.2	8.8
Voltage regulator	19	22	28	28	0	3	8.2	6.6
MEMORY CIRCUITS								
RAM 16K	23	29	24	18	0	6	7.1	7.7
RAM 64K	32	24	24	16	0	4	6.2	6.9
RAM 256K	14	33	29	19	0	5	7.5	8.6
ROM/PROM	5	33	29	33	0	0	8.3	9.5
EPROM	16	37	17	27	0	3	7.4	8.4
EEPROM	5	16	37	37	0	5	10.8	10.8
DISPLAYS								
Panel meters	0	32	47	16	5	0	8.3	8.0
Fluorescent	0	30	30	30	10	0	10.4	10.4
Incandescent	0	40	30	10	20	0	10.0	12.7
LED	18	41	26	11	4	0	5.6	6.8
Liquid crystal	0	33	44	17	6	0	8.3	9.6
MICROPROCESSOR ICs								
8-bit	9	43	29	14	0	5	6.9	8.5
16-bit	5	48	28	14	0	5	7.0	8.4
FUNCTION PACKAGES								
Amplifier	12	44	19	19	0	6	7.3	10.7
Converter, analog to digital	3	27	53	10	3	4	8.3	10.7
Converter, digital to analog	6	29	29	24	6	6	10.1	10.8
LINE FILTERS	20	33	20	20	7	0	7.2	8.9
CAPACITORS								
Ceramic	26	34	20	20	0	0	5.5	6.0
Ceramic monolithic	23	27	35	15	0	0	5.8	7.4
Ceramic disc	31	24	31	10	4	0	5.5	7.4
Film	22	44	22	12	0	0	4.6	7.6
Electrolytic	10	31	47	9	3	0	6.7	7.1
Tantalum	18	24	49	6	3	0	6.1	7.8
INDUCTORS	5	38	28	24	5	0	8.1	9.3

Source: *Electronics Purchasing* magazine's survey of buyers

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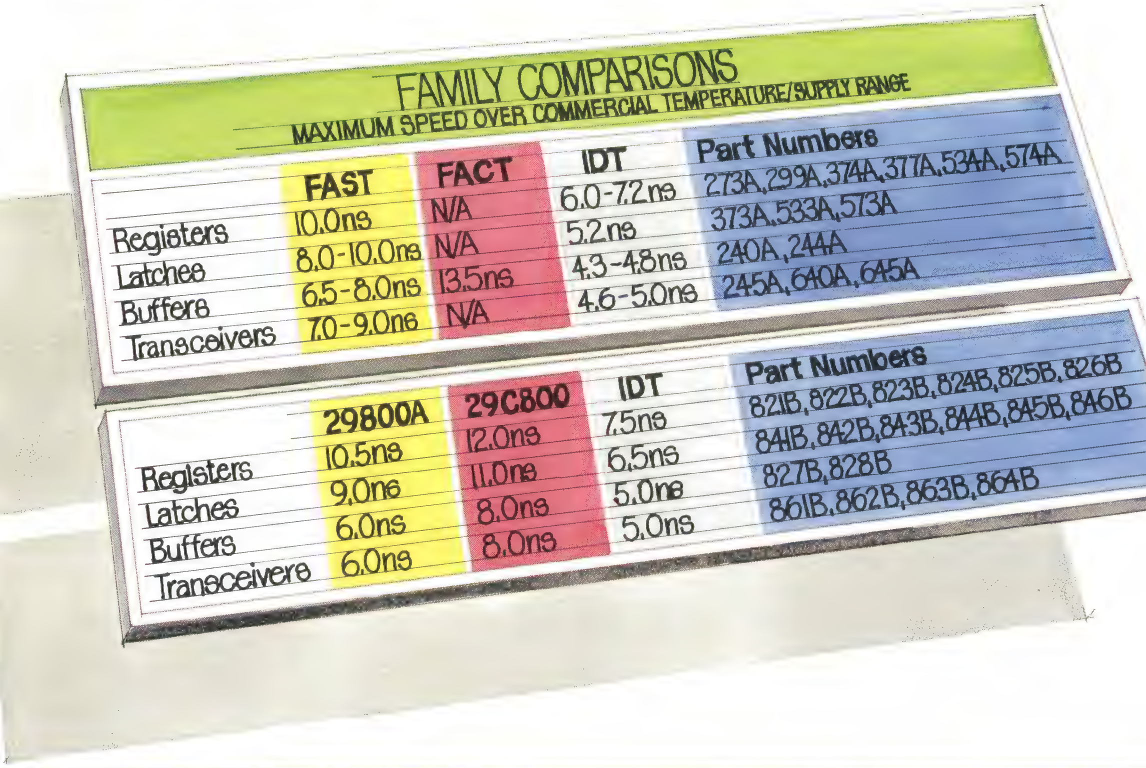

FAMILY COMPARISONS

MAXIMUM SPEED OVER COMMERCIAL TEMPERATURE/SUPPLY RANGE

	FAST	FACT	IDT	Part Numbers
Registers	10.0ns	N/A	6.0-7.2ns	273A,299A,374A,377A,534A,574A
Latches	8.0-10.0ns	N/A	5.2ns	373A,533A,573A
Buffers	6.5-8.0ns	13.5ns	4.3-4.8ns	240A,244A
Transceivers	7.0-9.0ns	N/A	4.6-5.0ns	245A,640A,645A

	29800A	29C800	IDT	Part Numbers
Registers	10.5ns	12.0ns	7.5ns	821B,822B,823B,824B,825B,826B
Latches	9.0ns	11.0ns	6.5ns	841B,842B,843B,844B,845B,846B
Buffers	6.0ns	8.0ns	5.0ns	827B,828B
Transceivers	6.0ns	8.0ns	5.0ns	861B,862B,863B,864B

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- ☐ **Outputs.** Com'l I_{OL} is 48 to 64mA. Com'l I_{OH} is –15mA.
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SPECIAL REPORT

DSP ICs

Choosing digital signal-processor chips isn't as difficult as it might seem. But beware: There are pitfalls along the way, from your first pencil sketch—where design subtleties await—to your implementation of an actual DSP task.

***New DSP chips** force engineers to pull together many hardware- and software-design techniques. (Photo courtesy Analog Devices Inc)*

JON TITUS, Senior Editor

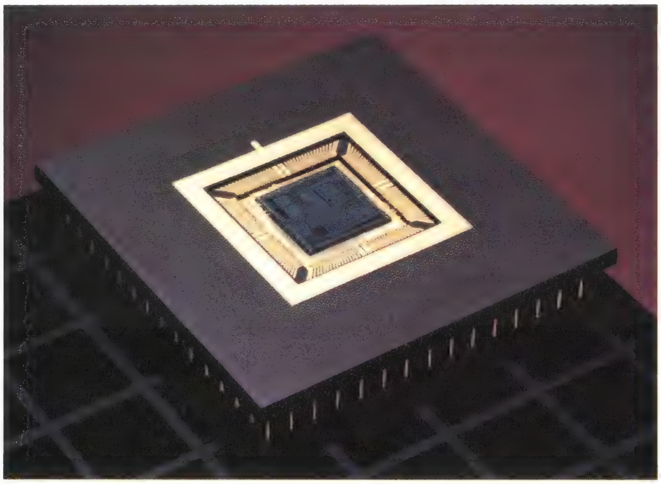
Most digital signal-processor (DSP) chips are very similar to general-purpose μPs, and your experience with the latter will serve you well when choosing and applying these devices. However, once you get past the simple interfacing tasks that involve external memories, host computers, and I/O devices, the similarities diminish. You need to know about memory structures, benchmark programs, pipelines, interrupts, and other topics that will influence your choice of a DSP chip.

The DSPs employ a Harvard-type architecture, in which the data and program memories are usually separate. Early DSP chips, such as Intel's now-obsolete 2920, NEC's μPD7720, and Texas Instruments' TMS32010, provide internal ROM that stores program steps. Newer DSPs, such as Analog Devices' ADSP-2100 and Zoran's ZR34161, require external memories for program storage. In fact, many of the new DSP chips also require external memory for data storage.

Although the DSP manufacturers seem to agree that memory spaces for instructions and data should be separate, they disagree on how to implement such memory structures. For example, DSPs from Motorola, Texas Instruments, and AT&T Technology Systems each provide one address and one data bus for all communication with such external devices as memory and I/O chips. On the other hand, Analog Devices, National Semiconductor, Oki Semiconductor, and Thomson Components-Mostek Corp provide separate buses that control separate data and instruction memories. The single-bus manufacturers state that simplicity is the key, while multiple-bus advocates state that their chips can deliver more information to the CPU in a given amount of time and thus have the advantage.

DSP chips adopt a Harvard-type architecture, which separates data and program memories and thus increases CPU throughput.

Generally following a Harvard-type architecture, Analog Devices' ADSP-2100 furnishes completely separate data, address, and control buses for data and program memories **(Fig 1).** The chip also addresses such I/O devices as A/D and D/A converters, but such devices must reside within the 16-bit data-memory space. The program-memory space stores as many as 16k 24-bit instructions. The chip's architecture diverges from the Harvard scheme in its ability to store data values within the program memory, though such data remains in its original 16-bit format. If you require additional space to store data, you can use the chip's program-memory address-valid ($\overline{\text{PMAV}}$) signal as a fifteenth address bit, thus expanding the program memory's address range to 32k addresses. You can't store instructions in the extra 16k-address space, however; it's for data storage only.



A typical DSP chip provides address, data, and control buses *that let it access external memories and I/O chips. The Signetics PCB5011 includes three address and data buses; it's packaged in a 144-pin pin-grid array.*

Mixing data and instructions in the ADSP-2100's program-memory space confers a speed advantage. For example, in a window-processing operation, the computer multiplies each value in a set of data by a coefficient it obtains from a table. After obtaining the multiply instruction from its program memory, the CPU independently and simultaneously fetches the raw data from the data-only memory and the coefficient from the program memory. Such a parallel-fetch operation speeds the window process.

Obtaining the two values from separate memory spaces is twice as fast as obtaining them from one memory space. However, the computer cannot maintain a high data-transfer rate for long; it must go back to the program memory for the next instruction after each multiplication occurs. To help overcome the instruction-fetch bottleneck, the ADSP-2100's CPU includes an instruction-cache memory that stores the previous 16 instructions that the CPU performed.

If you're running a loop with 16 or fewer instructions, the ADSP-2100 CPU obtains the instructions from the cache memory instead of refetching them from the

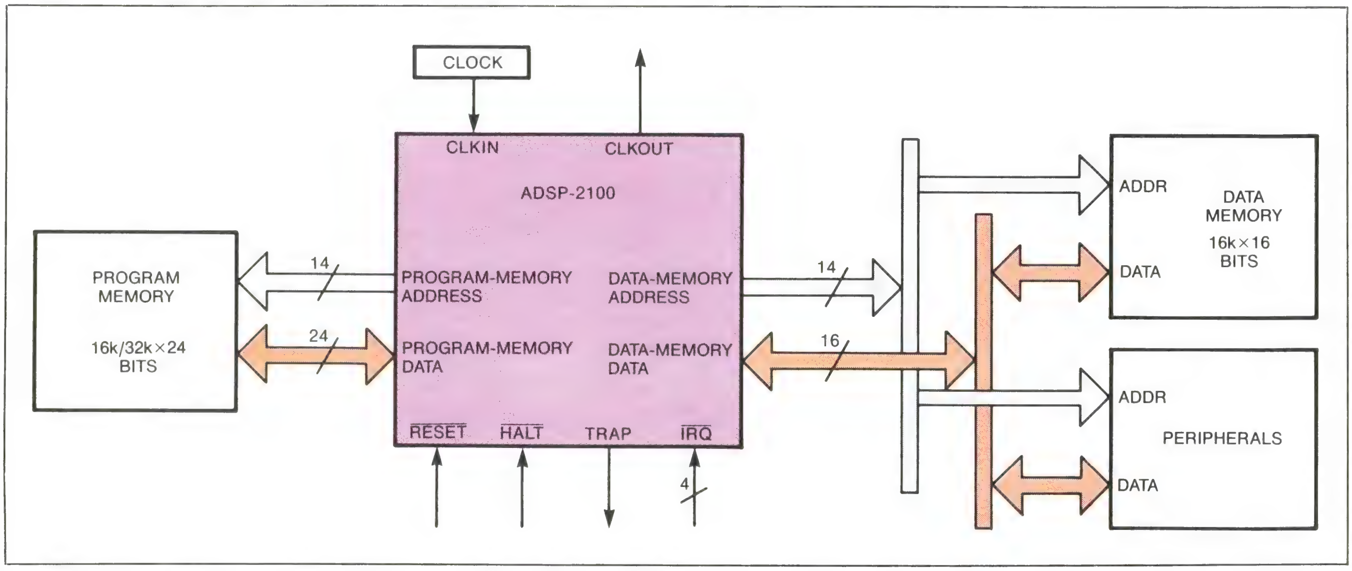


Fig 1—A typical DSP is a Harvard-type processor, *which provides separate buses for data and instruction storage. The ADSP-2100 from Analog Devices departs slightly from this scheme; it lets you address a 16k-word data memory and a 32k-word memory that stores both data and instructions.*

external program memory. The CPU still has to get the instructions into the cache, but it does so only once, during the first pass through the loop. After the second and subsequent passes through the loop, the CPU obtains its instructions from the cache. Consequently, the cache frees the bus of instruction-transfer operations and lets the CPU obtain data from both the data memory and the program memory during every CPU cycle.

Taking the multiple data-memory concept a step further, Motorola's DSP56000 chip (announced, but not in production) furnishes a pair of internal 256×24-bit data memories (X and Y) that you can expand externally to hold 64k values each **(Fig 2).** By furnishing independent data memories, you can partition your data into pairs of values arranged in an (x, y), (y, t), (real, imaginary), or other format. Unfortunately, the DSP56000 provides only one set of external buses, so

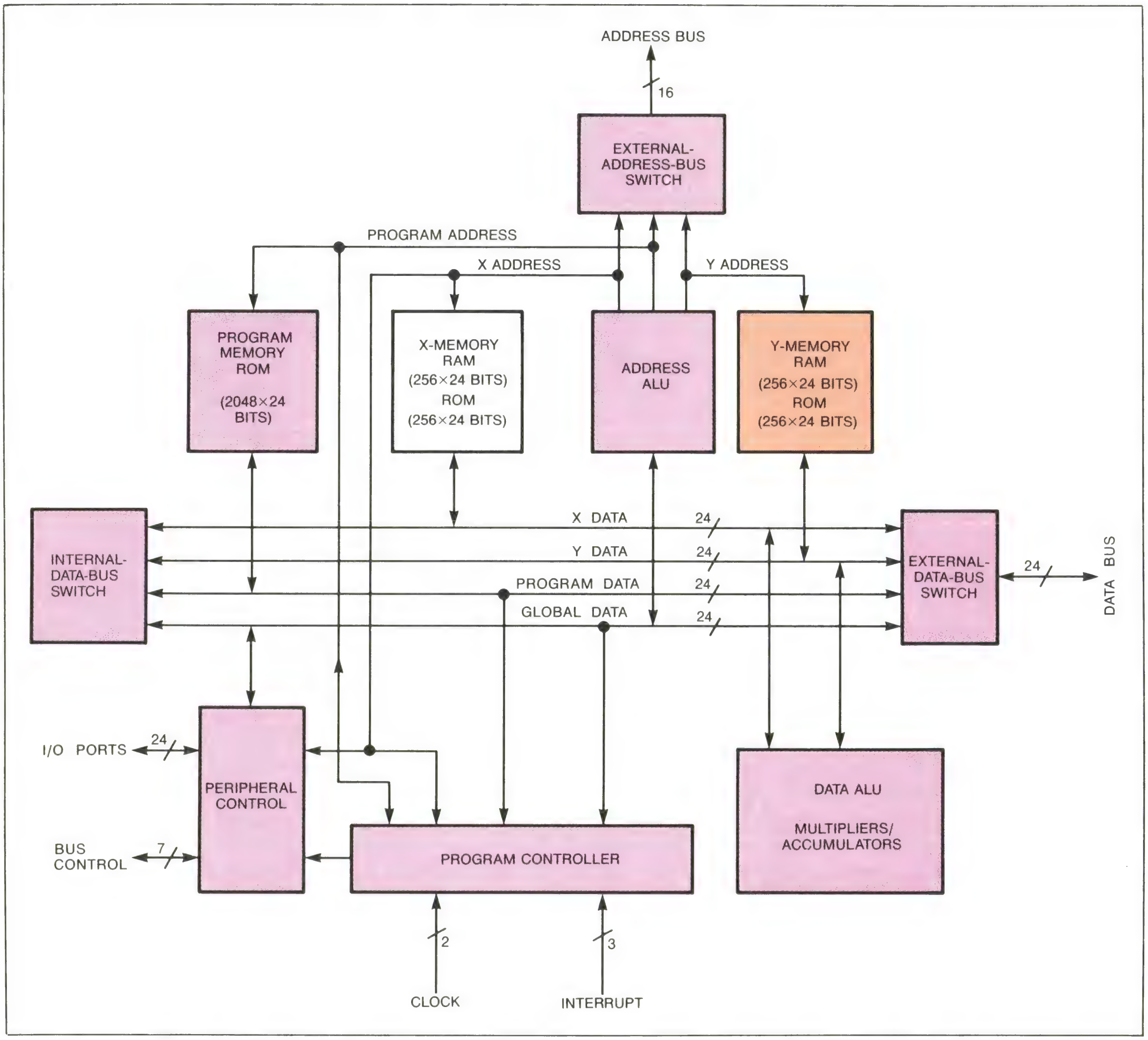


Fig 2—Two separate data memories *let Motorola's DSP56000 store and retrieve pairs of values for rapid processing. You can store (x, y), (y, t), (real, imaginary), or other pairs of data in the X and Y memories.*

Although you can expand external data and program memory, several DSP manufacturers create a bottleneck by forcing all transfers through a single set of buses.

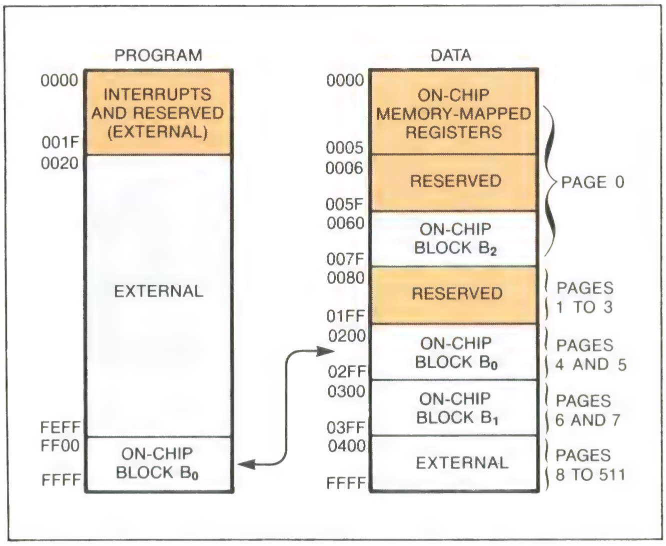


***Fig 3—A reconfigurable memory-address map** lets TI's TMS32020 move a 256-word block of RAM between the program and data memories under software control. When you move block B_0 to program memory, pages 4 and 5 in the data memory don't exist.*

the computer must access one set of memories at a time.

You can also expand the DSP56000's program-memory space externally to a maximum of 64k instructions. However, when the CPU must fetch an instruction and two values from external memories, you'll observe a 2-cycle delay in your program. If the memories require wait states, the delay will be longer.

DSP controls wait states internally

Instead of providing a ready-signal input pin of the type associated with general-purpose μPs that work with slow memories, the DSP56000 controls memory and I/O wait-state timing internally. A bus-control register (BCR), also called port A, lets you set the number of wait states that the CPU executes while it's transferring information to and from external devices. Because the chip performs four types of transfers—three for memories (X, Y, and program) and one for I/O devices—the CPU lets you program independent delays for each of the four transfer operations. Each wait state takes half an instruction cycle, and the BCR's delays range from zero to as many as 15 wait states for each type of device.

The DSP56000 provides circuits that let you set its address space in either a normal-expanded or a development mode. In the normal-expanded mode, the chip enables its internal 2k×24-bit program ROM, from which programs originate. The development mode disables the program ROM so that all program steps must originate from external resources. The development mode lets you substitute external memories for the chip's internal program ROM so you can test your software. You can also test software in the normal-expanded mode, but the development mode gives you access to the addresses that normally correspond to the internal ROM's space.

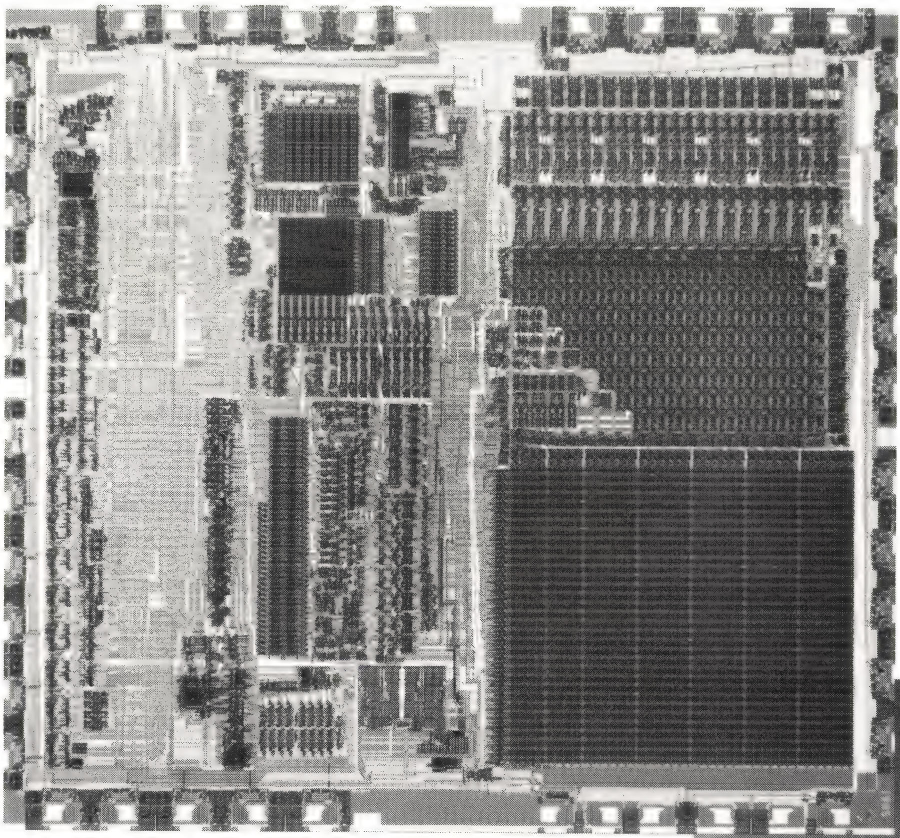
Instead of using external I/O pins to set its memory configuration, TI's TMS32020 chip lets your software dynamically reassign the chip's 256-word B_0 block of RAM to either program- or data-memory spaces **(Fig 3)**. Two instructions let you switch the memory block back and forth to suit special needs. You might, for example, store program steps in the block while it's part of data-memory space and then switch it to the program-memory space to run the program.

Two memory banks establish program- and data-storage areas for the AT&T DSP32 chip. The first 56k bytes constitute bank 0, while bank 1 addresses the subsequent 8k bytes. (Although the DSP32 operates on 32-bit values, AT&T specifies memory space in bytes.) For the chip to obtain its highest memory-access speed, the CPU must alternate between the two banks, although software may address either bank as necessary. Thus, while the CPU transfers data to or from one bank, it addresses the other and prepares for the next memory access. The overlapping of the memory-access cycles cuts the overall access time in half. Keep in mind that to take advantage of the higher speed you obtain from alternating between memory banks, you'll have to write programs that keep track of data that is divided between the two banks.

Because only the bank-0 address space is expandable off chip, external memory chips may operate twice as slowly as the on-chip memories; the CPU accesses them every other cycle. Because the DSP32's internal RAM is dynamic, however, the chip cannot wait for external memories or I/O devices that require long access times. You must use fast memories with this chip.

Taking a different approach to memory-access timing, the NEC μPD77230 divides its external memory into two sections: a 4k-address section for high-speed memories that require no wait states, and a 4k-address section for memory chips that require as many as three wait states. Both high- and low-speed memory operations occur in parallel with program execution.

Memory-access timing is subtle; keep this fact in mind when you're using a simulator, an emulator, or an evaluation board that lets you run test programs on a DSP. You might assume that your program will run at the chip's full speed, when in fact the DSP obtains its



Almost all DSP chips furnish internal RAM *that you can use to store data. The Zoran ZR34161 lets you save 128 complex values (real-imaginary pairs) on the chip. The chip also contains a sine-cosine look-up table in ROM.*

Software and a development board *from Zoran let you test a DSP and run your applications software on it. Most manufacturers support their DSP chips with a variety of software tools, sample programs, application notes, and technical data.*

data and instructions from slow external memory. When you test your software and your hardware-interface circuits on something other than your target system, be sure you know what timing restrictions, if any, apply.

In addition to high-speed memories that quickly feed the data and instructions to the CPU, most of today's DSPs include a pipeline that helps maintain high processing speeds. DSP chips aren't alone in using pipelines, of course; almost all high-speed computers rely on them for increased speed. The pipeline assures the CPU a steady stream of instructions that are already partially decoded and ready for execution by the time they reach the CPU. However, because a pipeline introduces a delay between the time the chip receives an instruction and the time it executes that instruction, handling a pipeline often proves troublesome for programmers.

For example, if a CPU with a 3-stage pipeline reads an instruction at time t, the instruction's results won't be available until time $t+2$ (where 2 is the number of cycles). When an instruction in AT&T's DSP32 chip specifies a memory-write operation, the result isn't available until four instructions later. Similarly, when a branch instruction tests for a condition, the operation that establishes the condition must occur four instructions prior to the test:

```
1  a0 = a0 + a1
2  az = a0 * az
3  ...
4  ...
5  if (condition) go to next
```

As a consequence, the program must calculate the value and establish the condition at line 1 that the instruction at line 5 tests.

Branch instructions can also cause problems for pipe-

By using an external ready signal or a programmable register, you can configure some DSP chips to operate with slow memories and peripherals.

lined processors. Again, consider the DSP32, which always executes the instruction that follows a branch operation—whether you want it to or not. To overcome the extra-instruction effect, AT&T recommends placing a no-operation (NOP) instruction directly after each branch instruction. Following one branch operation immediately with another one also leads to unpredictable results in NEC's µPD77230 DSP.

The pipeline in the Signetics PCB5010 and PCB5011 DSP chips varies from no stages or one stage for an elementary operation to as many as four stages for a complex operation. A typical complex operation includes one that reads an instruction, multiplies two values, accumulates a sum, and stores the sum in memory. You must study the assembly-language listing to know when the result from such an operation is

TABLE 1—COMPARISON OF DSP CHIP FEATURES

COMPANY	CHIP	TECHNOLOGY	PACKAGE	AVAILABILITY	SECOND SOURCE	MILITARY	MAXIMUM POWER DISSIPATION (W)
ANALOG DEVICES	ADSP-2100	CMOS	100-PIN PGA	SAMPLES NOW	NONE	YES	0.6
AT&T	DSP-32	NMOS	40-PIN DIP 100-PIN PGA	NOW	NONE	NO	2.7
FUJITSU	MB8764	CMOS	88-PIN PGA 84-PIN PLCC	NOW	NONE	EXTENDED TEMP	0.3
MOTOROLA	DSP56000	CMOS	88-PIN PGA 88-PIN PLCC	SAMPLES 1st QTR '87	NONE	NO	<1.0
NATIONAL SEMICONDUCTOR	LM32900	CMOS	172-PIN PGA 172-PIN PLCC	SAMPLES 4th QTR '86	NONE	YES	0.5
NEC	µPD7720	NMOS	28-PIN DIP	NOW	OKI, GOULD	NO	0.6
	µPD77C20	CMOS	28-PIN DIP 44-PIN PLCC	NOW	OKI, GOULD	NO	0.2
	µPD77230	CMOS	68-PIN PGA	SAMPLES 4th QTR '86	NONE	NO	1.7
OKI SEMICONDUCTOR	MSM6992	CMOS	132-PIN PGA	NOW	NONE	NO	0.4
PHILIPS/SIGNETICS	PCB5010	CMOS	68-PIN PLCC	SAMPLES 1st QTR '87	NONE	NO	0.5 TO 1
	PCB5011	CMOS	144-PIN PGA	SAMPLES 4th QTR '86	NONE	NO	0.5 TO 1
THOMSON/MOSTEK	TS68930	NMOS	48-PIN DIP	1st QTR '87	NONE	EXTENDED TEMP	3
	TS68931	NMOS	84-PIN PLCC	SAMPLES NOW	NONE	EXTENDED TEMP	3
TEXAS INSTRUMENTS	TMS32010	NMOS	40-PIN DIP 44-PIN PLCC	NOW	GI	YES	1
	TMS320C10	CMOS	40-PIN DIP 44-PIN PLCC	NOW	GI	YES	0.4
	TMS32011	NMOS	40-PIN DIP	NOW	NONE	NO	1
	TMS32020	NMOS	68-PIN PGA	NOW	NONE	NO	1.2
	TMS320C25	CMOS	68-PIN PLCC	SAMPLES 4th QTR '86	NONE	YES	0.5
ZORAN	ZR34161	CMOS	48-PIN DIP	NOW	NONE	1st QTR '87	0.5

KEY:
MAC = MULTIPLIER/ACCUMULATOR
GI = GENERAL INSTRUMENT CORP
LUT = LOOK-UP TABLE

available. To simplify programming, you can switch the Signetics chips to their nonpipelined mode, but each instruction then requires two instruction cycles. The longer cycle time may be a small price to pay, because you won't have to pad a program with extra instructions to stretch it so that results are available immediately from each operation.

Not all of today's DSPs require a pipeline. Results in the DSP56000 are available immediately after the CPU completes an instruction.

Although pipelines and memory architectures help speed DSP tasks, the chips can't process data without communicating with I/O chips and, in some cases, with host computers. Several chips rely exclusively on external I/O ports, while others have combinations of internal parallel and serial ports. You'll find one of the most

INTERNAL RAM ADDRESSES	INTERNAL ROM (BITS)		EXTERNAL MEMORY (BITS)		LOW-POWER MODE	ON-CHIP PARALLEL I/O	ON-CHIP SERIAL I/O
	PROGRAM	DATA	PROGRAM	DATA			
NONE	NONE	NONE	32k×24	16k×16	YES	NO	NO
1024	512×32 (SHARED)	512×32	14k×32	14k×32	NO	YES	YES
256	1k×24	NONE	1k×24	1k×16	YES	NO	NO
512	2k×24	512×24	64k×24	128k×24	YES	YES	YES
NONE	NONE	NONE	64k×28	128k×16	YES	YES	YES
128	512×23	512×13	NONE	NONE	NO	NO	YES
128	512×23	512×13	NONE	NONE	NO	NO	YES
512	2k×32	1k×32	4k×32	8k×32	NO	YES	YES
256	1k×32	NONE	64k×32	64k×22	NO	NO	NO
256	987×40	512×16	NONE	NONE	NO	NO	NO
256	NONE	NONE	1k×40	512×16	NO	NO	NO
256	1280×32	512×16	64k×32	4k×16	NO	NO	NO
256	NONE	512×16	64k×32	4k×16	NO	NO	NO
144	1536×16	NONE	4k×16	NONE	NO	NO	NO
144	1536×16	NONE	4k×16	NONE	NO	NO	NO
144	1536×16	NONE	NONE	NONE	NO	NO	YES
288 256 DATA/PROG	NONE	NONE	64k×16	64k×16	NO	NO	YES
288 256 DATA/PROG	4096	NONE	64k×16	64k×16	YES	NO	YES
128 COMPLEX VALUES	NONE	256-POINT COSINE LUT	64k×16	64k×16	NO	NO	NO

(more chip features on next page)

TABLE 1—COMPARISON OF DSP CHIP FEATURES *(Continued)*

COMPANY	CHIP	DMA	DATA TYPE	DATA-VALUE LENGTH (BITS)	MAC INPUT PRECISION (BITS)	MAC OUTPUT PRECISION (BITS)
ANALOG DEVICES	ADSP-2100	YES	INTEGER	16	16×16	40
AT&T	DSP-32	YES	FLOATING POINT	24-BIT MANTISSA 8-BIT EXPONENT	32×32	40
FUJITSU	MB8764	YES	INTEGER	16	16×16	26
MOTOROLA	DSP56000	YES	INTEGER	24	24×24	56
NATIONAL SEMICONDUCTOR	LM32900	YES	INTEGER	16	16×16	32
NEC	μPD7720	YES	INTEGER	16	16×16	32
	μPD77C20	YES	INTEGER	16	16×16	32
	μPD77230	NO	FLOATING POINT	24-BIT MANTISSA 8-BIT EXPONENT	24×24	47-BIT MANTISSA 8-BIT EXPONENT
OKI SEMICONDUCTOR	MSM6992	YES	FLOATING POINT	16-BIT MANTISSA 6-BIT EXPONENT	SEE COMMENTS	SEE COMMENTS
PHILIPS/SIGNETICS	PCB5010	NO	INTEGER	16	16×16	40
	PCB5011	NO	INTEGER	16	16×16	40
THOMSON/MOSTEK	TS68930	YES	INTEGER	16 OR 32	16×16	32
	TS68931	YES	INTEGER	16 OR 32	16×16	32
TEXAS INSTRUMENTS	TMS32010	NO	INTEGER	16	16×16	32
	TMS320C10	NO	INTEGER	16	16×16	32
	TMS32011	NO	INTEGER	16	16×16	32
	TMS32020	YES	INTEGER	16	16×16	32
	TMS320C25	YES	INTEGER	16	16×16	32
ZORAN	ZR34161	YES	INTEGER	16 (SEE COMMENTS)	17×17 (SEE COMMENTS)	17

KEY:
MAC = MULTIPLIER/ACCUMULATOR
GI = GENERAL INSTRUMENT CORP
LUT = LOOK-UP TABLE

flexible I/O arrangements on the DSP56000, which supplies 24 I/O lines divided between two I/O ports (B and C).

The 15 I/O lines at port B perform general-purpose parallel I/O operations, or they serve as a bidirectional communication and control bus that links the DSP with a host computer. You use the nine lines at port C as general-purpose parallel I/O connections, or you can use them to form two serial ports. The serial ports support a serial-communication interface (SCI) and a synchronous-serial interface (SSI), both of which control peripherals. The SCI lets the DSP communicate with other devices that use a character-oriented asynchronous protocol. The SSI interface is a subset of Motorola's SPI protocol, which supports low-cost peripherals and μPs.

National's LM32900 DSP (announced but not yet available) will also provide on-chip I/O ports—two serial ports and two parallel ports. One serial port receives 16-bit data, while the other serial port transmits 16-bit values. Similarly, one parallel port delivers 16 bits while the other port obtains 16-bit values from external devices. Both parallel ports rely on FIFO buffers that are 16 words deep. The serial and parallel ports all have control and clock lines so that external devices can regulate their operations.

Decode ports carefully

Texas Instruments' TMS32010 chip contains no I/O ports, but it addresses as many as eight 16-bit I/O ports, which are external to the chip. In order to address the I/O ports, the chip must decode a 12-bit address and combine it with either a read or a write-enable signal. You must take care when designing the part of your system that decodes output-port addresses, because the OUT instruction and the table-

MULTIPLY/ ACCUMULATE TIMING (nSEC)	INTERRUPT LEVELS	STACK LEVELS	EXTERNAL BUSES	PRICE (QTY)	COMMENTS
125	4	16	2 DATA 2 ADDR	$337	32k-ADDRESS EXTERNAL PROGRAM MEMORY INCLUDES 16k ADDRESSES OF DATA STORAGE
122	1	EXTERNAL MEMORY	1 DATA 1 ADDR	$298	NON-HARVARD ARCHITECTURE; DATA AND INSTRUCTIONS DO NOT REQUIRE SEPARATE ADDRESS
100	2	1	1 DATA 1 ADDR	$99 (1000)	
97.5	4	EXTERNAL MEMORY	1 DATA 1 ADDR	SEE TEXT	
200	6	15	2 DATA 1 ADDR	SEE TEXT	
250	1	4	1 DATA	$12 (1000)	77P20 PROVIDES ON-CHIP EPROM
250	1	4	1 DATA	$15 (1000)	
150	2	8	1 DATA 1 ADDR	$100 (1000)	
100	3	8	2 DATA 2 ADDR	$250	MAC I/O OPERATIONS TAKE PLACE IN 22-BIT FLOATING-POINT FORMAT
250	1	5	1 DATA 1 ADDR	$200	INTERNAL RAM PROVIDES 32 INSTRUCTION LOCATIONS
250	1	5	3 DATA 3 ADDR	$200	
160	1	1	1 DATA 1 ADDR 1 SYSTEM	$157	256 ROM LOCATIONS RESERVED FOR SELF-TESTING ROUTINES; OPERATES ON REAL OR COMPLEX DATA
160	1	1	2 DATA 2 ADDR 1 SYSTEM	$277	INTERRUPT GOES TO THE HOST COMPUTER
320	4	4	1 DATA 2 ADDR	$10 (1000)	
400	4	4	1 DATA 2 ADDR	$12 (1000)	
400	4	4	1 DATA 1 ADDR	$11.50 (1000)	
200	4	4	1 DATA 1 ADDR	$30 (1000)	
100	8	8	1 DATA 1 ADDR	$37 (1000)	
100	1	EXTERNAL MEMORY	1 DATA 1 ADDR	$700	MULTIPLIER OPERATES ON REAL AND IMAGINARY DATA SIMULTANEOUSLY; MULTIPLIER ROUNDS RESULTS TO 17 BITS

write instruction (TBLW) both generate write-enable signals. To avoid address conflicts, the chip should uniquely decode all 12 address bits for each output port and avoid doing table-write operations to the output-port addresses.

In contrast, the TMS32020 provides an internal serial I/O port that lets you transmit and receive either 8- or 16-bit information. If you choose not to use the serial ports, you can use their associated registers to store 16-bit values. The chip also addresses as many as 16 parallel I/O ports. Unlike the older TMS32010, the TMS32020 provides a signal that specifically controls the parallel I/O ports and avoids conflicts between memory and I/O-port addresses.

DSP chips must synchronize or coordinate their signal-processing tasks with the information flowing to and from I/O devices. Most available DSP chips provide an interrupt that lets external devices demand immediate service. This interrupt-servicing architecture, however, is reminiscent of the architecture of early μPs: Most of the chips have a limited number of internal stack locations that save return addresses when you process interrupts. Even so, an internal stack has an advantage over one in external memory: It's fast.

The ADSP-2100 has features that make it particularly useful for interrupt-driven tasks. When the chip accepts an interrupt signal, it stores its program counter (PC) on a 16-level stack, and it stores its status on a 4-level stack. Because the status stack contains only four levels, you can't nest interrupt-service routines more than four deep. The ADSP-2100 responds to an interrupt in two cycles, but the interrupt-service software may require additional time for housekeeping tasks, such as checking the loop- and down-counter stacks if the interrupt routine needs to use those counters.

Pipelines speed processing by assuring the CPU a steady flow of partially decoded instructions.

The ADSP-2100 supplies a stack-status register that lets your program check the condition of the chip's four stacks. If a stack overflows, it refuses to save any new data and it maintains the old data instead. The old data is considered more important than the new data, because you can probably recover the new data from somewhere else in the computer. Until you do a processor-reset operation, the chip's stack-overflow status bits remain set.

Because manufacturers are aiming their DSPs at real-time data-processing tasks, it's surprising that only the ADSP-2100 provides context switching. This function handles interrupts by making a quick exchange of working registers for a set of standby registers. After processing the interrupt, the CPU exchanges the registers again, thus restoring the information that the interrupt had stopped the CPU from processing. Switching the registers after an interrupt-service routine completes its task saves the interrupt information so that it's ready when the next interrupt occurs.

The DSP56000 provides two types of interrupts—fast and slow. If you store a 2-word or two 1-word instructions at the start of the interrupt-service routine, the CPU performs a fast interrupt that simply inserts one or two instructions into the normal program flow. Don't use instructions that modify flag or status bits in a fast-interrupt routine: The CPU doesn't save or restore status bits during fast-interrupt operations. You can't interrupt the CPU again while it's processing a fast interrupt.

If a DSP56000 interrupt-service routine starts with a jump-to-subroutine instruction, the CPU enters a long-interrupt state, which is like a conventional μP interrupt. The CPU saves the PC, clears registers, and performs other housekeeping tasks. The CPU also clears its interrupt-priority level, thus preventing further interrupts at the same level or at lower levels.

The Motorola DSP56000 provides a stack-error flag bit that the CPU sets when you try to push data onto a full stack or read data from an empty stack. A stack-error condition causes a software interrupt that forces the CPU into an exception state. It's your responsibility to provide exception-processing software that detects and corrects stack errors.

The interrupt structure in the Thomson TS68930 and TS68931 chips is a bit unusual for DSP chips. Instead of receiving an interrupt from an external device, the chips generate an interrupt that controls communications with a host computer through a set of mailbox registers. Zoran's ZR34161 chip also generates an interrupt that regulates information flowing between a host computer and the DSP.

A CPU's pipelined architecture can cause interrupting devices to suffer delays in getting to their service routines. For example, when the μPD77230 receives an interrupt signal, it completes its current operation and saves the value of the PC on its stack. Although another instruction is already waiting in the pipeline, the CPU must not execute it. Instead, it executes a NOP instruction and then jumps to the start of the interrupt-service routine. After the interrupt-service routine completes its operation, the CPU must refill the pipeline with instructions so that it can restart its operations at the instruction that was in the pipeline when the interrupt occurred.

Math formats offer choices

Interrupts, memory architectures, and I/O control are important factors in selecting a DSP, but you'll also need to decide how you want the chip to process your data. Consequently, another of the decisions you'll have to make is whether to use integer math or floating-point math. Floating-point math is familiar—it's available on pocket calculators and most computers—and AT&T, Oki, and NEC offer DSPs that operate with floating-point values. The remaining manufacturers' chips operate with integer values. Although floating-point math offers a large dynamic range and reduces rounding errors, fixed-point math offers enough dynamic range to solve most DSP problems.

Fixed-point math has some disadvantages, however. Math operations that the chips do directly, such as addition and multiplication, yield results that contain more bits than the computer can store. For example, the result of multiplying two 16-bit values is a 32-bit value that you'll have to round or truncate to 16 bits before you save it. As an alternative to this procedure, you can temporarily save the intermediate 32-bit result in an accumulator at the multiplier's output if you are going to use it in a subsequent math operation. By saving intermediate results in registers within the chip, you avoid some rounding problems. You round the final result of sequential operations rather than each intermediate result.

Rounding can lead to instabilities in infinite-impulse-response (IIR) filters and other systems that use feedback or recursion. Rounding becomes particularly important in small numbers, for it can lead to extremely large changes in a value. For example, rounding 2.51 to

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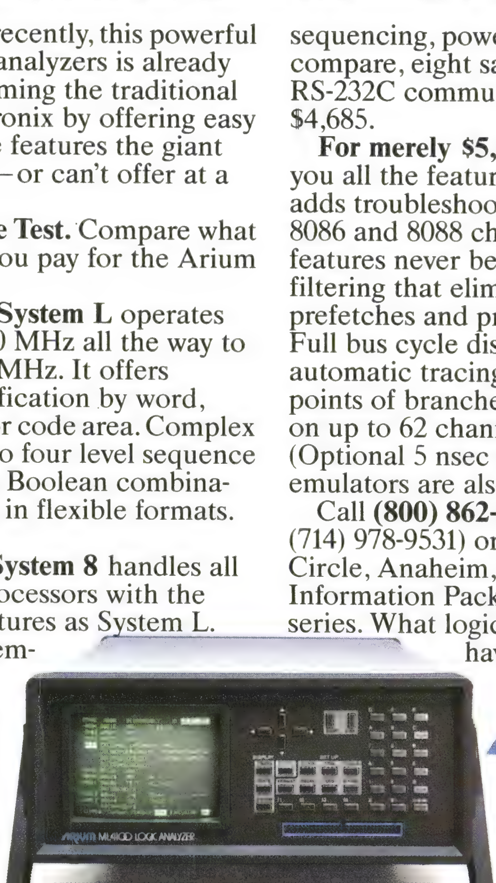

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3 produces a 16% error, and rounding very small numbers can produce a result of 0. There's a big difference between dividing a value by a small number or by 0. In floating-point computers, the rounding error doesn't depend on the magnitude of the value you're rounding.

Consider block floating-point math

Before you jump to a floating-point chip, you might consider block floating-point math, which offers a hybrid, floating/fixed-point solution. Computers represent block floating-point values by assigning a common exponent to a block of integer values. You still manipulate the exponents and mantissas as integers, but depending on the results of a math operation, the CPU adjusts the integers in the block and the block's exponent as necessary. Analog Devices' ADSP-2100 chip provides exponent-derivation hardware that lets you compare the exponent associated with a block of numbers with the exponent of a new result, updating the block exponent as needed.

Keep in mind that floating-point operations take longer than fixed-point ones. The CPU must normalize results and perform other housekeeping tasks. In a lengthy routine, the extra time adds up quickly. Also, most peripherals, such as A/D and D/A converters, operate with integer values and require only so much resolution. You should therefore take care not to overspecify precision. Before you choose a math format, consider the task and review the precision you'll need for starting, intermediate, and final values.

To demonstrate the data-processing abilities of their DSP μPs, manufacturers provide benchmark DSP programs that are supposed to let you compare operations on one chip to similar operations on others. You may have a sense of déjà vu, particularly if you followed the benchmark wars among μP manufacturers in the late '70s and early '80s. Unfortunately, the benchmark situation hasn't changed: Benchmarks remain subjective. For example, assertions of high-speed operation may apply only to special cases, such as tasks that fit all their data within the DSP's internal RAM. So take speed specifications and benchmarks with a grain of salt.

The fast Fourier transform (FFT) is a popular benchmark program, and most manufacturers list the execution speed of at least one FFT routine. Although an FFT program seems like a good benchmark, because it involves moving and processing a lot of data, not all FFT routines are the same, nor are FFT benchmark results. For example, the FFT routine may operate on 64 data points, 1024 data points, or some number in between. The algorithm may use radix-2 or radix-4 operations, and it may be a straight-line program or one that runs in a loop.

Although the FFT routine for Signetics's PCB5010 chip includes windowing operations, which take extra time, the program processes only 256 values. Perhaps it's a coincidence that the chip's repeat instruction limits you to 256-pass loops.

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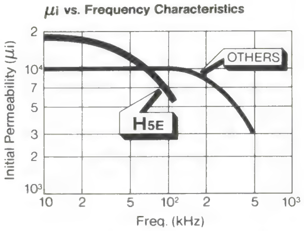

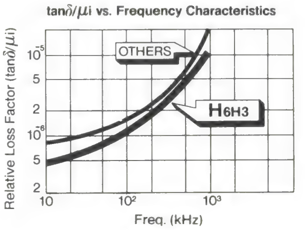

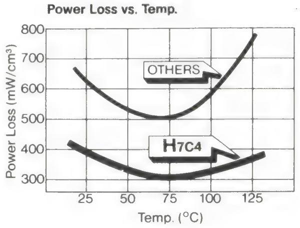

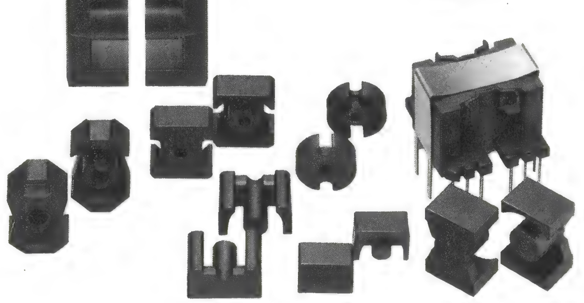

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Also, benchmarks may show only part of a complex problem. In graphics data processing, pixel convolutions require nine multiplication operations per pixel. However, typical illustrative routines usually don't show address manipulations, nor do they show the special operations that account for image-boundary conditions.

Accept no phantom chips

Before deciding on a DSP, be sure that the manufacturer is delivering DSP chips, or that their production is imminent. Although the National LM32900 and the Motorola DSP56000 have been announced, don't expect to see samples before late 1986 or 1987. Motorola does not provide an introductory price, except to say that chips in a plastic package should sell for under $50 in 1988. National Semiconductor expects to offer OEM quantities of its chip at $90 to $100.

Unfortunately many engineers put too much trust in preannouncements, treating them as a declaration that the chips will be available at a given date. Even when chips are available, it is good policy to identify a second source. Sadly, few of the DSP manufacturers have second sources for their chips, although many are now working to engage other semiconductor manufacturers as alternative suppliers. Remember that you're not buying just chips, you're buying a complete product that includes field-engineering support, applications information, technical data, seminar programs, software, and evaluation boards or development systems. When evaluating DSP chips, be sure you're getting the complete product that answers your needs. **EDN**

Acknowledgement

Dr Amnon Aliphas of DSP Associates (Newton, MA) provided much of the information contained in the DSP-chip comparison table.

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2. Professional Program Session Record No 18, "Programmable Single-Chip Digital Signal Processors," Mini/Micro Northeast, Boston, MA, May 1986.

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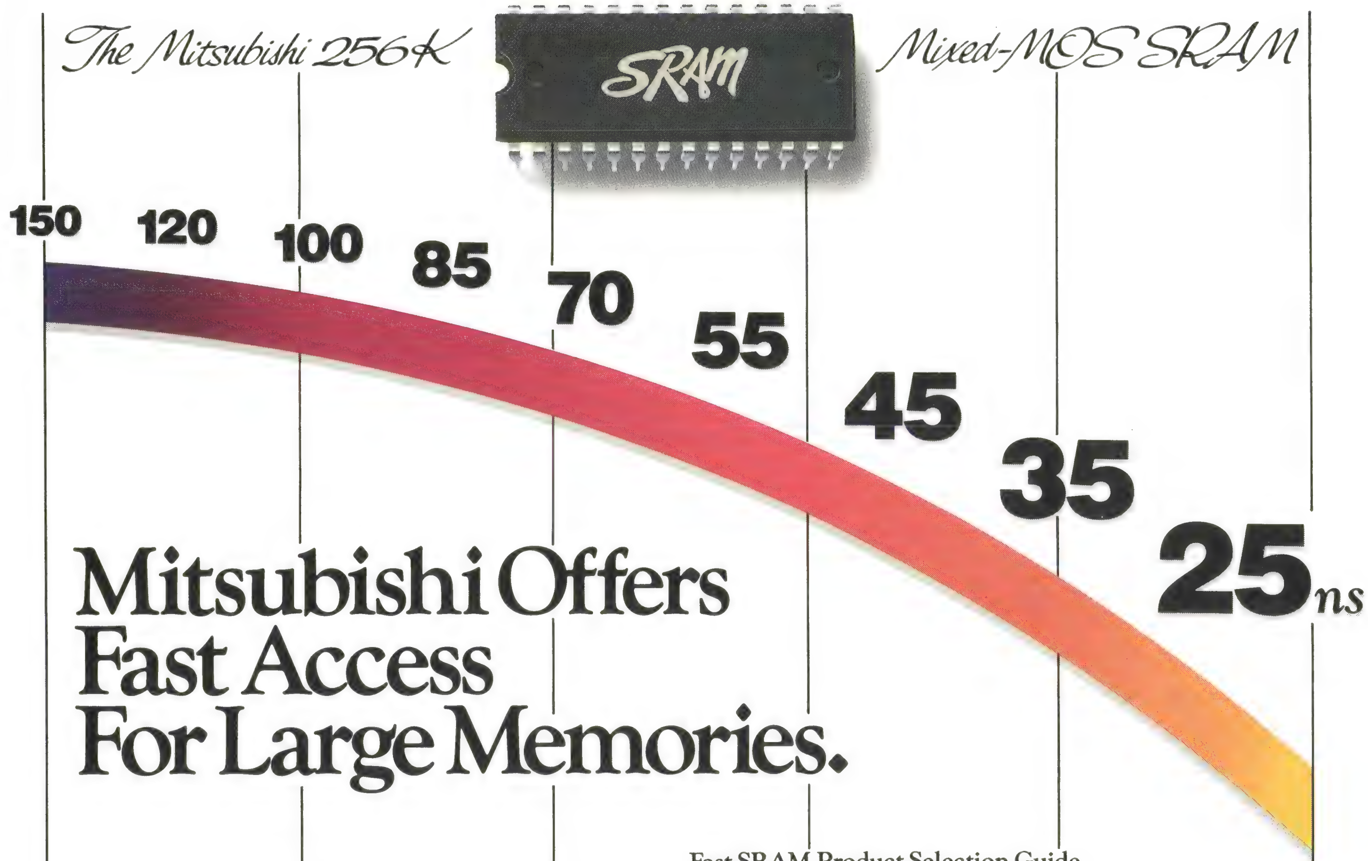

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M5M5178*	8K x 8			•	•						• 28 PIN (300 mil wide & 600 mil wide)		• 28 PIN
M5M5179*	8K x 9			•	•						• 28 PIN (300 mil wide only)		• 28 PIN
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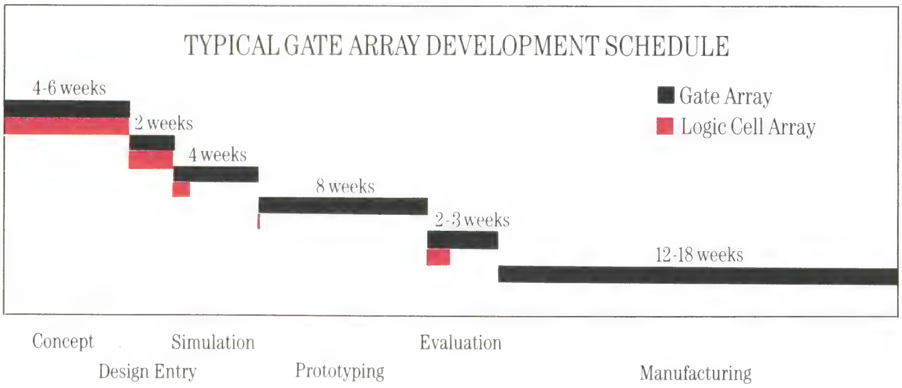

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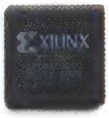

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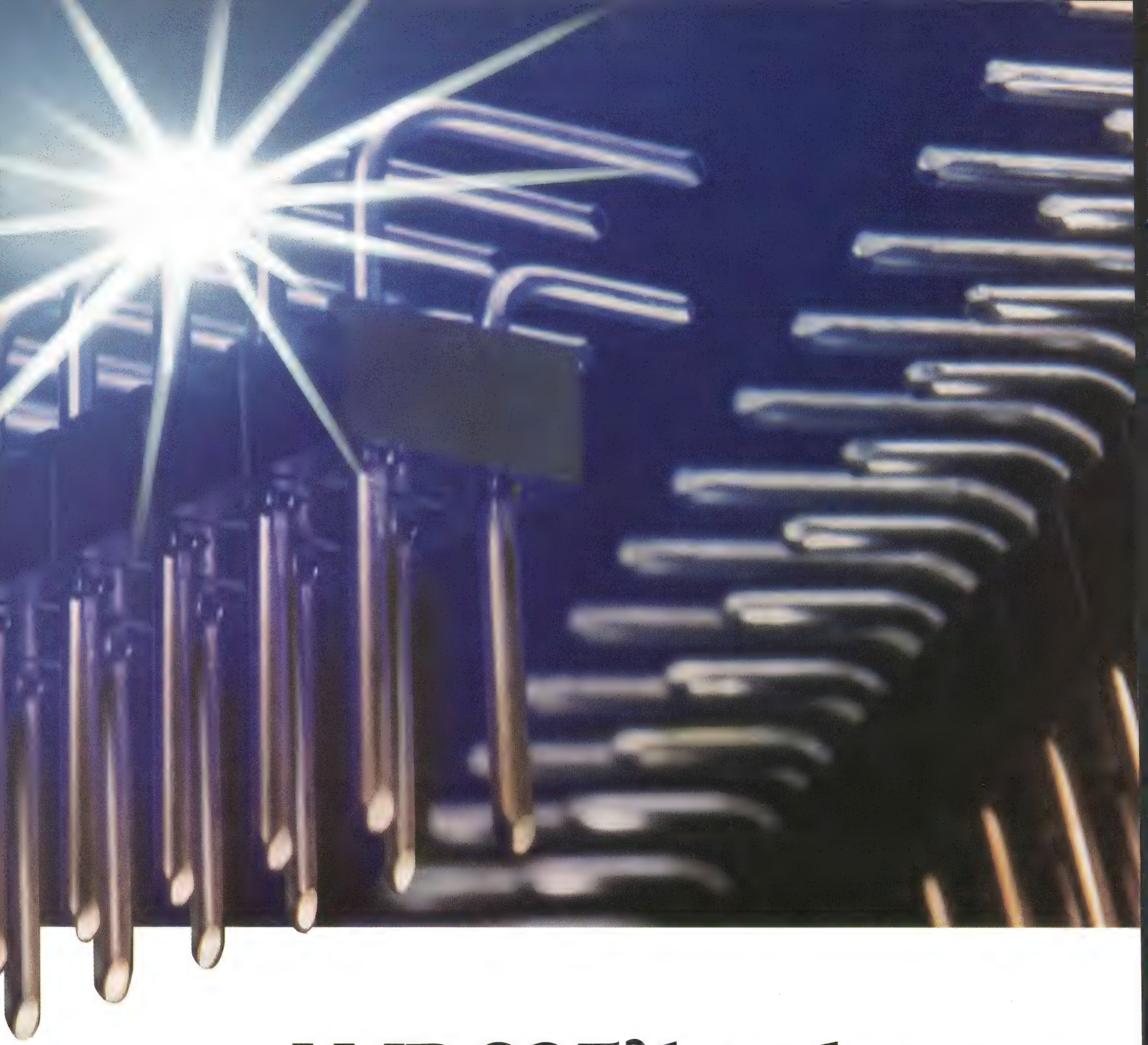

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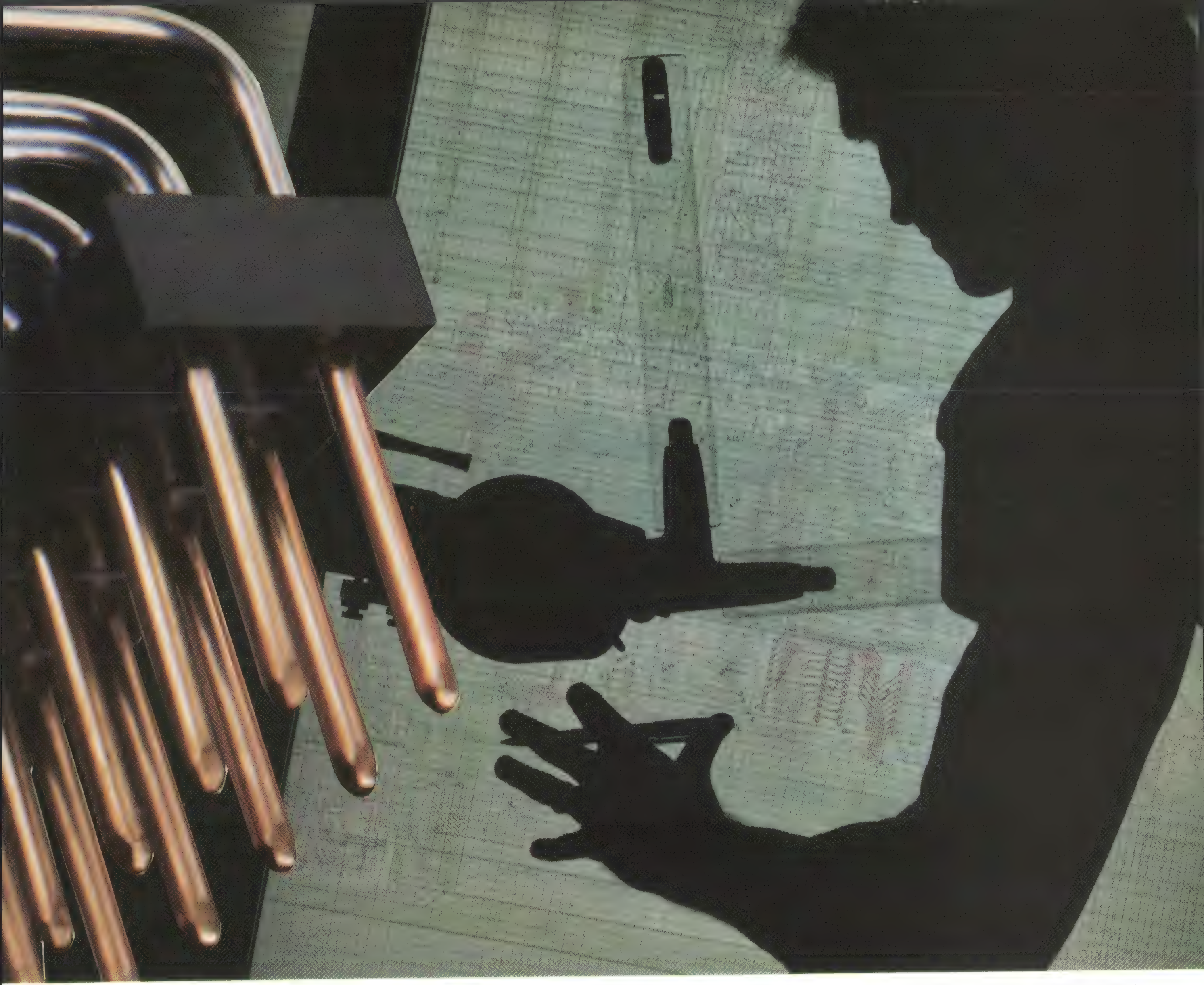

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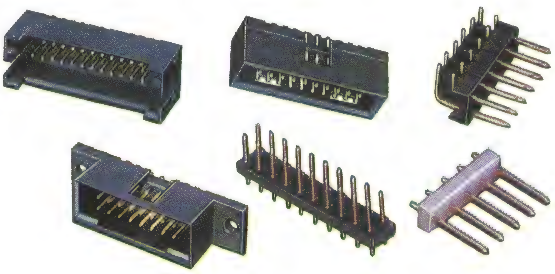

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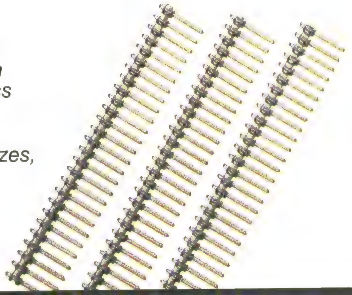

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Synchronous V/F converter aids linearity in data acquisition

By using a synchronous V/F converter (SVFC), you can design analog-input systems that have greater linearity than that attainable by using asynchronous V/F converters or A/D converters. In this article, first in a 2-part series, you'll become acquainted with V/F converters in general and the AD651 SVFC in particular.

Larry DeVito, *Analog Devices Semiconductor*

A voltage-to-frequency converter provides an easy and inexpensive way to convert analog signals to digital form. V/F converters that use internal one-shot multivibrators to set their scale factor, however, are subject to drift and nonlinearities. A synchronous V/F converter (SVFC) uses an external clock signal and thus minimizes drift and nonlinearities. Such a device proves useful in a variety of A/D applications, but you need to fully understand an SVFC's characteristics and specs.

Before delving into the operating theory of the AD651, consider the device's salient features. It's a monolithic synchronous V/F converter that operates at clock frequencies as high as 4 MHz and specs a maximum linearity error of 200 ppm. At lower clock frequencies, linearity approaches 20 ppm. If you apply a 1-MHz clock, gain drift can be as low as 25 ppm/°C. You can operate the device either from one supply or in the more traditional dual-supply mode; the supply voltage can be as low as 12V or ±6V.

The AD651 SVFC can also accept either positive or negative input voltages; gain error is 0.5% max. In addition, the device is calibrated for positive current inputs, for which maximum gain error is 1%. A one-shot controls the width of the frequency-output pulses. Note that this one-shot doesn't enter into the data-conversion process but simply drives the open-collector output: In some applications, it's desirable that the output pulse be shorter than the period of the clock. For example, driving an opto-isolator typically requires a significant amount of current, and you might need a very short pulse width to save power.

The output-frequency pulses are synchronous with the input clock; that is, the output pulses can only occur on the rising edges of the clock. The width of the pulses is controlled by a one-shot but can be no longer than the period of the input clock. This synchronization greatly simplifies the design of the digital portions of a data-acquisition system. Because the output pulses can arrive only at certain instances, the system can perform other tasks simultaneously. The SVFC uses the charge-balance method, so it retains the usual advantages expected of a V/F converter: high resolution and high noise rejection.

The simplest use of a V/F converter involves counting frequency-output pulses over a gate period to measure frequency. You can gain maximum benefit from the

SVFC's architecture if you derive the gate period by dividing the clock signal's frequency by an integral number. In this case, it isn't even necessary for the clock frequency to be temperature stable. Because the gain of the SVFC is proportional to the clock frequency, and because the gate time is inversely proportional to the clock frequency, the total number of pulses during the gate time (for a given input voltage) will remain constant with changes of the clock frequency.

Explanation of operation helps

Fig 1a shows a block diagram of the AD651 configured as an SVFC; **Fig 1b** shows various circuit waveforms. The input resistor connected to the integrator's summing junction transforms voltage to current, and an internal feedback current exactly balances this input current. The feedback appears as short, accurately timed bursts of current—that is, as precisely defined packets of charge. The required number of charge packets, each accompanied by one pulse of the output frequency, depends on the amplitude of the input signal.

Because the number of charge packets delivered per unit of time is a function of the input signal's amplitude, a linear voltage-to-frequency transformation occurs. The familiar up-and-down integrator output, typical of the charge-balance technique, is evident in **Fig 1b.** A positive input signal causes the integrator output to ramp downward. After the integrator output crosses the comparator's threshold and the output of the AND gate goes high, nothing happens until a negative edge of the clock comes along to transfer the information to the output of the D flip-flop.

At this point, the clock level is low, so the latch does not change state. When the clock returns high, the latch output goes high and drives the switch to reset the integrator. The internal reference current is now connected to the integrator's summing junction and, because this current is larger than the input signal, the current flow in the integrator capacitor reverses and the integrator's output voltage ramps upward. At the same time, the latch drives the AND gate to a low output state. On the next negative edge of the clock, the low output state of the AND gate transfers to the output of the D flip-flop; then, when the clock returns high, the latch output goes low and drives the switch back into the integration mode.

At the same time, the latch drives the AND gate to a

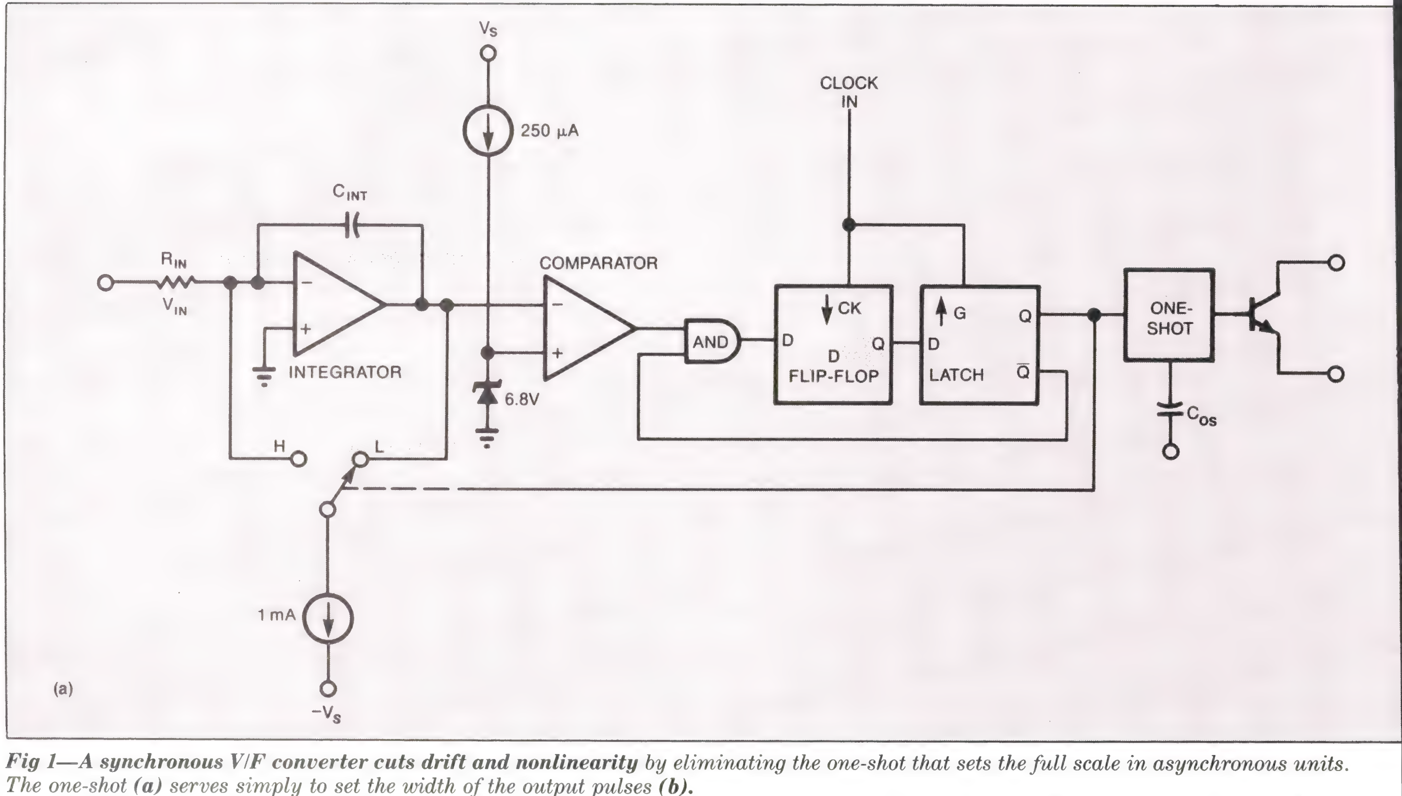


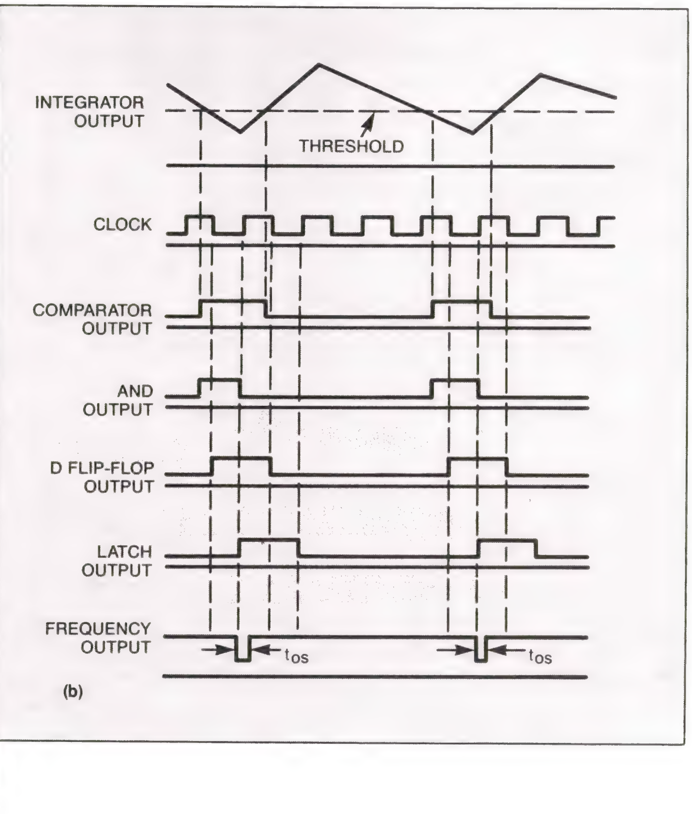
Fig 1—A synchronous V/F converter cuts drift and nonlinearity *by eliminating the one-shot that sets the full scale in asynchronous units. The one-shot **(a)** serves simply to set the width of the output pulses **(b)**.*

A synchronous voltage-to-frequency converter can provide much lower frequency drift than asynchronous units.

mode in which it will truthfully relay the information presented to it by the comparator. Each pulse is only one clock period long, so the full-scale output frequency is equal to half the clock frequency. At full scale, the current-steering switch spends half its time on the summing junction; thus, the circuit can balance an input current of 0.5 mA. In the case of an over-range input, the output of the integrator's op amp will drift off in the negative direction and saturate, and the output of the comparator will remain high at all times. The logic circuits then simply settle into a divide-by-2 operation, and the output frequency is exactly half the clock frequency. The transfer function of the SVFC is

$$f_{OUT} = \frac{V_{IN}}{20V} \times f_{CLOCK} = \frac{I_{IN}}{1\ mA} \times f_{CLOCK}.$$

Because the reset pulses applied to the integrator are exactly one clock period long, only a variation of the symmetry of the switching speed with temperature can cause drift. Of course, if the reference current changes with temperature, then the scale factor of the SVFC will also change. However, a buried-zener reference and wafer-level laser trimming impart good temperature stability to the internal current. Because every reset pulse is identical to every other (the clock gates all of them, so dielectric absorption can't cause the duration of a pulse to be influenced by the length of time since the last pulse), the AD651 SVFC produces a very linear voltage-to-frequency transfer function.



The number of pulses of the output frequency during a given period of time is proportional to the average value of the input signal over that period. If the input signal has been contaminated by the addition of noise that has a mean value of zero (60-Hz power-line hum, for example), then the SVFC can completely reject the noise. This repetitive-noise situation usually occurs with capacitively or inductively coupled noise. You must set the time period over which the average is taken such that it equals a whole number of cycles of the interfering hum.

You can easily use a counter to set this time period by making the gate time equal to one or more periods of the power-line frequency. Note that if the input voltage becomes negative, the current delivered to the summing junction will reverse direction and will still flow through the integrating capacitor. As long as the integrator's operational amplifier remains active, a continuous integration of the input signal occurs, and you're assured of noise rejection.

If the input signal becomes negative during the integration period, then the output voltage of the integrator will ramp upward, away from the comparator threshold. This occurrence is only a transient situation—eventually the signal must become positive, and the integrator output will ramp down and trigger the comparator. (For more information about the noise-integration properties of the charge-balance V/F converter, see **Ref 1**.)

Choose a capacitor

The value of the integration capacitor should be 0.02 μF; this element has no effect on the transfer relation but merely determines the amplitude of the sawtooth signal coming from the integrator. If you expect a large amount of normal-mode interference (more than 0.1V), and the clock frequency is less than 500 kHz, you should use an integration capacitor of 0.1 μF. (The value of the comparator's threshold voltage also has no effect on the transfer relation; it sets the dc voltage around which the integrator's output voltage oscillates.)

The dielectric absorption of the integration capacitor used with the AD651 is of some concern because the average voltage seen by the capacitor changes slightly

Voltage-to-frequency converters that use charge-balance techniques effectively nullify repetitive noise (for instance, 60-Hz hum) that stems from outside sources.

as a function of frequency. Polypropylene is the preferred capacitor type. Defects in the integrator capacitor can create problems for the system designer. For example, consider the situation in which you wish to squelch an AD651 by applying a negative input voltage. This action causes the integrator's output to rise to the positive-supply voltage and saturate.

The integrator capacitor will then soak at a voltage equal to the supply potential, and when the SVFC comes out of this standby mode, the integrator capacitor will remember its previous situation and slowly release absorbed charge as it soaks at its new average voltage. The charge being given up by the integrator capacitor represents a leakage and contributes directly as an input error. The result is that the output frequency will not immediately be stable but will slowly creep to a final value as the integrator capacitor forgets its past. (You can find more information about dielectric absorption by consulting **Ref 2.**)

In **Fig 1b,** you can see that the period between the output pulses is constrained to be an exact multiple of the clock period. Consider an input current of exactly one-quarter the value of the reference current. In order to achieve a charge balance, the output frequency will equal the clock frequency divided by 4—one clock period for reset and three clock periods of integration, as shown in **Fig 2.** If the input current increases by a very small amount, the output frequency should also increase by a very small amount.

Initially, however, no output change is observable, and the output frequency continues to run at one-quarter the clock frequency, thereby delivering an average of 250 μA to the summing junction. Because the input current is slightly larger than this 250 μA, charge accumulates in the integrator, and the sawtooth signal starts to drift downward. As this drift occurs, the comparator-threshold crossing takes place earlier and earlier in each successive cycle until, finally, a whole cycle is lost.

When this cycle is lost, the integration phase lasts for two periods of the clock instead of the usual three. Thus, among a long string of divide-by-4s, an occasional divide-by-3 occurs; the average output frequency is

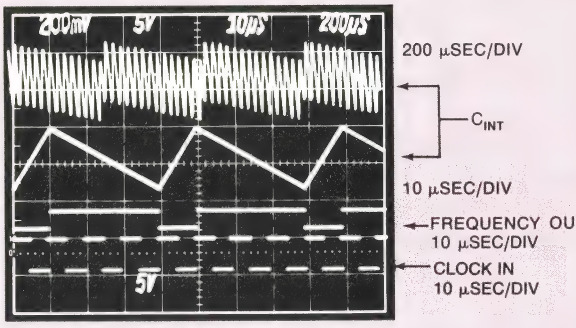


*Fig 3—**The SVFC integrator's output is a sawtooth wave** that has a sawtooth envelope. You can consider the SVFC's output to be a frequency that undergoes phase modulation—that is, it accumulates phase at 2πf rads/sec.*

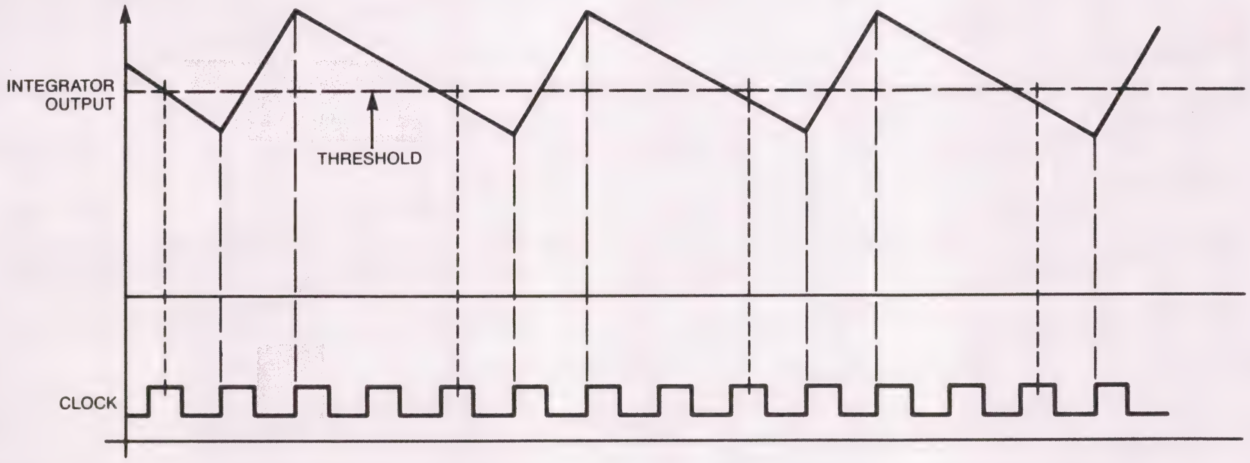


*Fig 2—**Input current equal to one-quarter the reference current** produces these integrator-output waveforms in the circuit of **Fig 1.** The output frequency equals the clock frequency divided by 4—one clock period for reset and three periods of integration.*

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When you use an SVFC, the practical way to extract data from the output bit stream is to count pulses, as opposed to an asynchronous VFC's ratio-counting method.

very close to one-quarter of the clock's repetition rate, but the instantaneous frequency can be very different. During this cycle time, the signal at the output of the integrator is a sawtooth wave having an envelope that's also a sawtooth, as shown in **Fig 3**.

Alternative approach is feasible, too

Another way to view this synchronicity is to consider that the output is a frequency (approximately one-quarter the clock's frequency) that has undergone phase modulation. You can think of a constant frequency as accumulating phase at a constant rate of 2πf rads/sec. Hence, the average output frequency, which is slightly in excess of a quarter of the clock's, will require phase accumulation at a certain rate. However, because the SVFC is running at exactly one-quarter of the clock frequency, it will not accumulate enough phase, as you can see in **Fig 4**.

When the difference between the required phase (average frequency) and the actual phase equals 2π, a step in phase occurs, and the deficit is made up instantaneously. The output signal is a steady carrier that's been phase modulated by a sawtooth signal. The period of the sawtooth phase modulation is the time required to accumulate a 2π phase difference, and the amplitude of the phase modulation is 2π.

The result of this synchronicity is a limited rate at which you can extract data from the bit stream produced by the SVFC; counting output pulses from the SVFC is thus the most practical answer. When you use

Synchronization cleans up a V/F converter's act

A versatile building block in modern data-acquisition systems, the charge-balance voltage-to-frequency converter (VFC) accepts an analog input and produces a series of output pulses having a frequency proportional to the average amplitude of the input. In its simplest application, the V/F converter counts pulses for a fixed gate time; in order to make a measurement of *n* bits, the gate time must be long enough to accumulate 2^n pulses when the V/F converter is operating at full scale. Because the input signal undergoes continuous integration, the properties of a charge-balance V/F converter are guaranteed monotonicity, high resolution, and rejection of hum and noise.

Voltage-to-frequency conversion is slower than other techniques for data conversion but offers more flexibility; it's a trivial task to trade off between conversion speed and measurement resolution by using a computer-controlled pulse counter. Moreover, you can achieve measurement resolution far greater than that possible with any other data-converter IC. You can extend resolution almost indefinitely by simply waiting long enough to accumulate a sufficient number of output pulses.

The ultimate resolution of a V/F converter is limited by noise and drift and not by architectural constraints. Finally, a V/F converter offers a cost advantage when high resolution—rather than high speed—is of primary importance. Furthermore, if many signals need simultaneous monitoring, the cost savings can be quite dramatic.

The synchronous voltage-to-frequency converter (SVFC) is a variation of the charge-balance V/F converter. You must apply an external clock signal to the SVFC, and the period of this clock signal serves as the primary timing reference, making the scale factor proportional to this external clock frequency. In an ordinary charge-balance V/F converter, gain drift with temperature can originate from both the dc reference and the one-shot.

Even if the one-shot were perfect, the temperature coefficients of its capacitor would still introduce errors. The SVFC completely eliminates the one-shot; only the dc-reference errors remain, and you can make them very small. Improved linearity is another advantage of the SVFC architecture; because the clock controls each reset period, the periods are all identical.

In V/F converters using a one-shot, the duration of a reset pulse is influenced slightly by the length of time elapsed since the last reset pulse, and this influence results in nonlinearity. In the SVFC, the pulses of the output frequency are generated in phase with the input clock—that is, a rising (or falling) edge of the input clock initiates and terminates the reset period.

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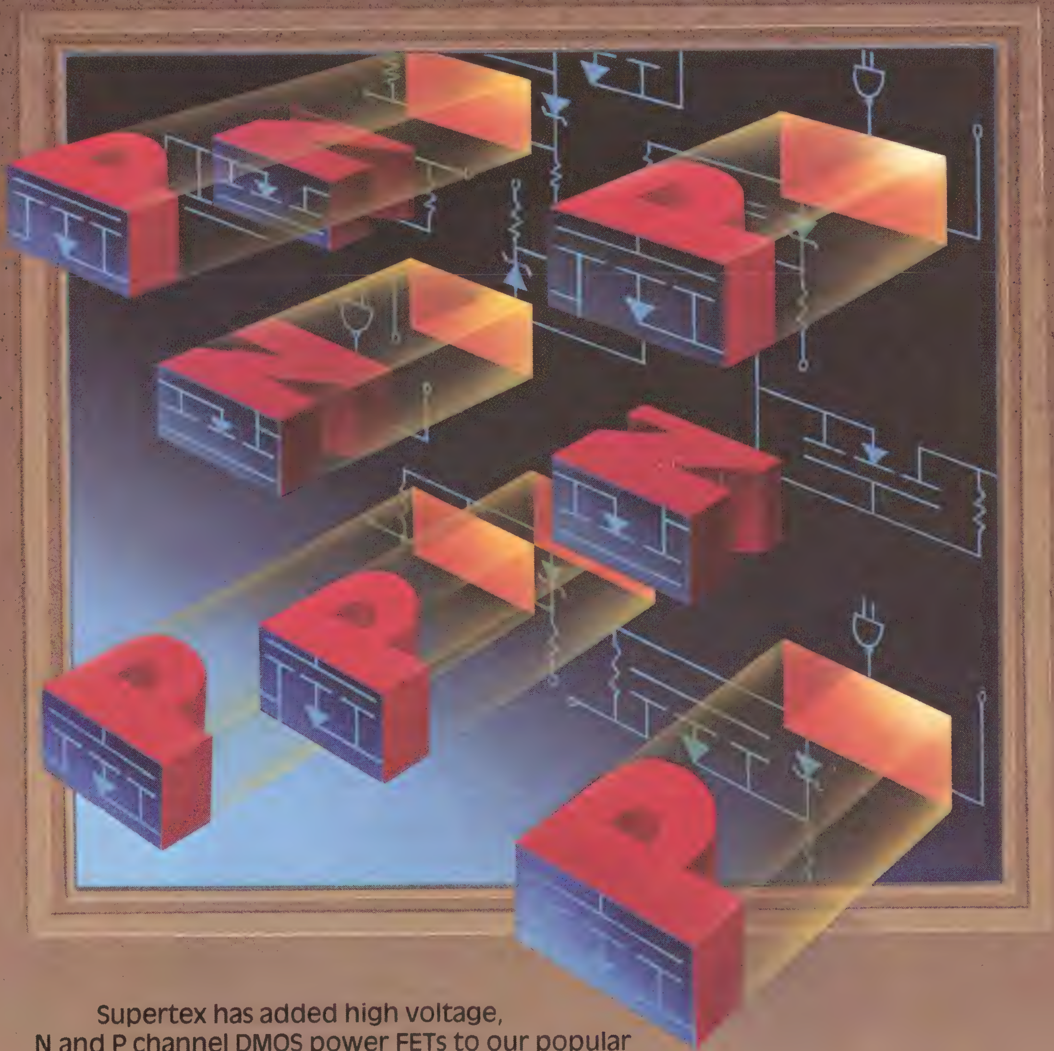

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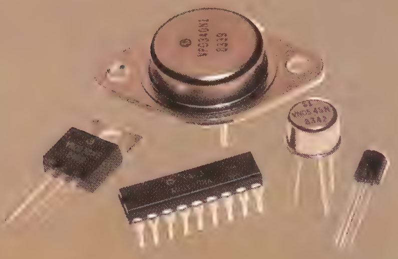

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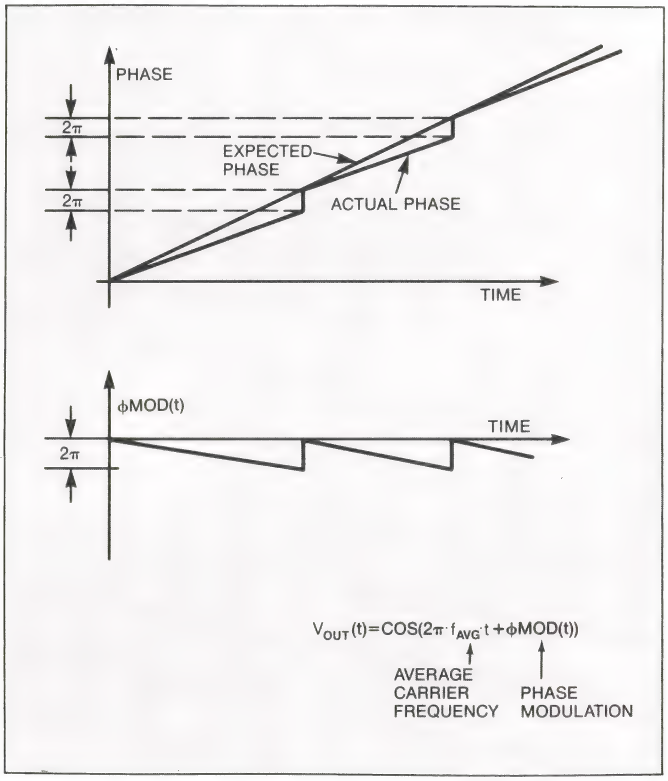
Although the value of the integrating capacitor you use with an SVFC isn't critical, you should take care to choose units having low dielectric absorption.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2π
2π
EXPECTED PHASE
ACTUAL PHASE
TIME
φMOD(t)
TIME
2π
$V_{OUT}(t)=COS(2\pi \cdot f_{AVG} \cdot t+\phi MOD(t))$
AVERAGE CARRIER FREQUENCY
PHASE MODULATION

Fig 4—When the difference between the expected and actual phase is 2π, *a step in phase accumulation occurs in the SVFC, and the output signal's phase jumps to the value it should have. The result is a steady carrier that undergoes phase modulation by a sawtooth wave.*

normal (asynchronous) frequency, you can use faster methods for measuring frequency than simply counting pulses. In ratio counting, for example, the period of time required to accumulate an integral number of signal cycles is easy to determine (with great resolution). You simply count pulses from a high-frequency clock, which is gated by the signal to be measured. You must then numerically compute the result by dividing the two counts.

Jitter of the frequency under measurement limits the resolution obtainable by using ratio counting. However, this technique will not work with an SVFC because the phase modulation described earlier results in a large amount of jitter in the frequency. If you performed the ratio counting over an interval of time that didn't include any steps of the sawtooth phase modulation of **Fig 4,** then the result would be exactly one-quarter of the clock frequency—and this answer isn't correct.

If you performed the ratio counting over a short interval of time that happened to include one of these phase steps, then the result would also be wrong. The only way you'd obtain a correct answer is if the counting interval happened to be equal to the period of the sawtooth phase modulation. However, this period isn't fixed, but changes constantly with the signal.

You now have an idea of how a synchronous voltage-to-frequency converter can serve as a low-drift, high-resolution analog-conversion device. Part 2 (which will appear in the November 13 issue) will explain how to interpret some salient specs of the AD651 SVFC and will present three practical applications for the device: as a signal multiplexer, as an isolated analog front-end circuit, and as an analog multiplier. **EDN**

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Author's biography

Larry DeVito is a design engineer at Analog Devices Semiconductor in Wilmington, MA. An MIT graduate, he also worked for MIT in the Crystal Physics Laboratory at the Center for Materials Science and Engineering, developing sputtered x-ray phosphors. Prior to joining Analog Devices, Larry was an IC designer at Sprague Electric. He enjoys reading and gardening in his spare time.

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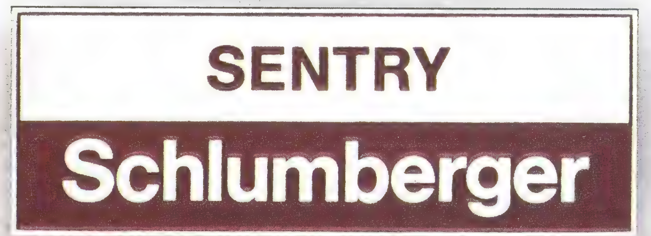
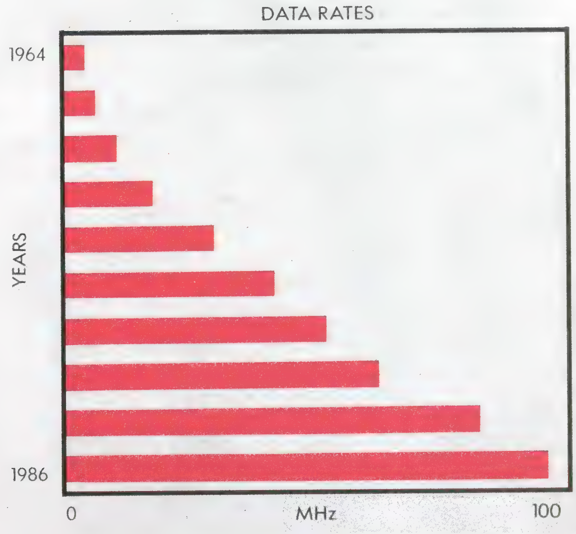


History repeats itself.



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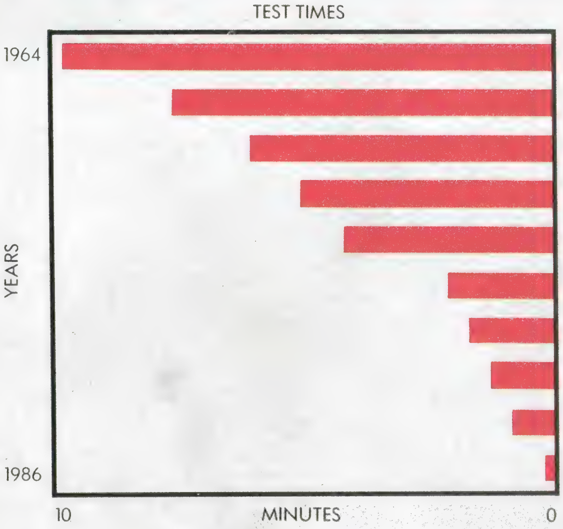

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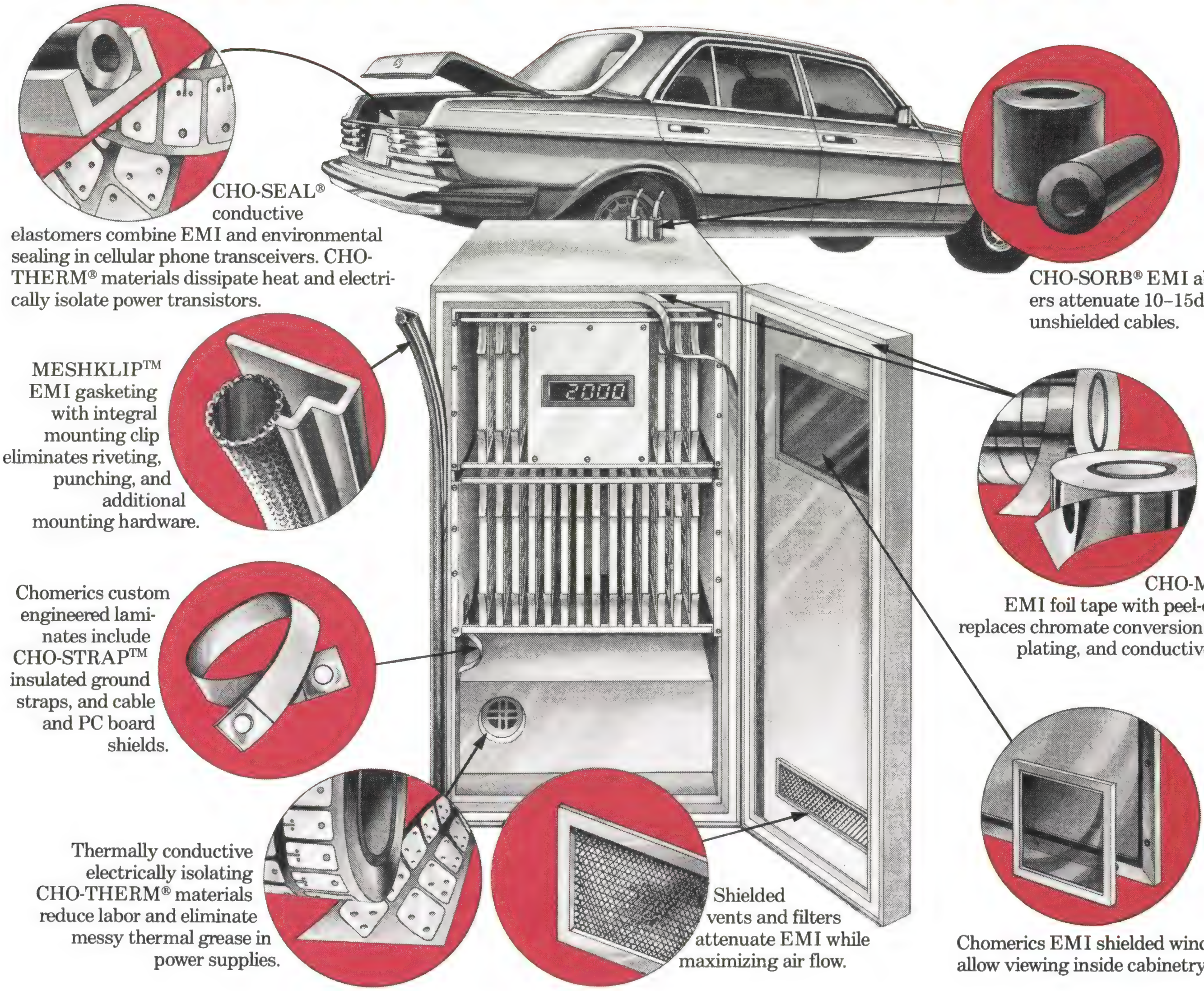

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CIRCLE NO 163

Touchscreen displays suit multifarious applications

After 10 years of technical improvement and cost reduction, touch-sensitive screens have achieved price and performance levels that compare favorably with other computer-input devices. Given that, and the ultimate simplicity of the technology itself—the pointing of a finger—it's puzzling that more applications don't make use of it.

John Javetski, *Santa Clara, CA*

As touchscreen technology has matured, resistance to it has shifted from system design engineers to end users and ergonomics experts. Decade-old technical questions about parallax and durability problems, attenuated brightness, and false triggering are being answered and are giving way to debates on ease-of-use issues like availability of touch-activated applications software and the aesthetics of touching greasy screens.

Vendors, on the whole, agree that touchscreen applications fall into two broad categories: those in which the touchscreen is the sole computer-interface vehicle, and those in which the touchscreen complements a keyboard or mouse or other peripheral input device.

The first category, with few exceptions, embraces those applications that represent the long-term future of touchscreen technology. All these applications assume that the end user is computer-shy—even though that may not in fact be the case—and therefore employ touchscreens as the most painless and simple, if not the most efficient, interface technique. Included in this category are public database-access systems like information kiosks; automotive trip computers, environmental controllers and engine-control systems; educational and commercial-training systems; interactive video systems based on emerging videodisk technology; and point-of-purchase or electronic shopping systems.

This category also encompasses applications that use a touch-sensitive display screen as the sole computer interface to speed or simplify a computer's operation by an industrial technician. This class of applications is characterized by a need to make the computer execute a series of complex, nonrepetitive tasks quickly and accurately. An example is medical instrumentation, where hospital personnel touch a monitor to quickly reconfigure a diagnostic system to display blood pressure, then heart rate, then body temperature. Another example is process-control systems, where touchscreens are replacing complex banks of switches.

A third subset of the category of touch-only applications is one that, so far, hasn't been developed much. Here, a touchscreen would replace a keyboard to prevent hackers from tampering with or accessing the contents of a secure database. Such a configuration might find favor in military and financial applications

In process-control systems, touchscreens are replacing complex banks of switches.

where computer access must be provided, but must be limited to some degree.

The second category of touchscreen-technology applications—those in which a touchscreen serves as an adjunct to a keyboard or a mouse—has potentially explosive, but unproven growth possibilities. Into this category fall two large markets: office and design automation. The application variables here include the degree of computer literacy of the end user, as well as his or her ergonomic preferences. Some typists, for example, refuse to remove their hands from a keyboard to operate a mouse or touchscreen, whereas others seem more amenable to switching off between input devices if doing so will improve their productivity.

In design automation, end users are intimately familiar with keyboards and mice but are also willing to accept new technology that might make them work faster and more productively. A touchscreen is less efficient than a keyboard or keypad for entering numerical data, but once the data is in the system, a touchscreen—supported by tailored software—might just be the fastest way to manipulate it.

If you build computers for end use in any of the above markets and think that touch-sensitive input might improve your product, you'll have to decide which touchscreen technology best fits the needs of your customers. Perhaps more than in other fields, the environmental and operational characteristics of the intended application will determine which technology is most appropriate.

A tale of three technologies

You can choose from three different types of touchscreens: capacitive, resistive-membrane, and optical. (A fourth—discussed in the **box,** "A sound approach to touchscreen technology"—has just been revived.) The three types are sold as kits containing a frame that installs under the bezel of a particular monitor or flat-panel display, plus the electronics needed to sense and locate the position of a touch and report it back to the host computer over an RS-232C link.

Capacitive touchscreens, sold by Interaction Systems, Kiel, MicroTouch Systems, and Touch Technology, are glass faceplates, or overlays, onto which is sputtered a thin resistive-capacitive coating like indium tin oxide (ITO) and an insulating layer of silicon dioxide. All capacitive touchscreens sense the change in capacitance that results when a conductive probe like a finger or special stylus (not a gloved finger or pencil eraser) touches the screen.

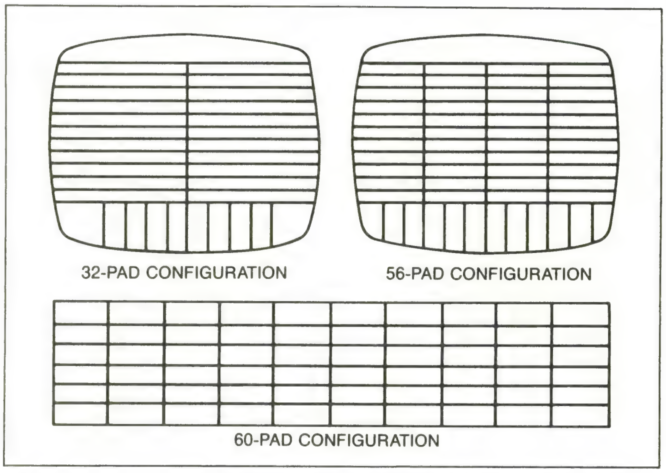


Fig 1—To exploit the economics of scale, *vendors of discrete capacitive touchscreens sell standard-configuration products like these three offerings from Touch Technology. If your applications can work with such an arrangement of touch pads, you can avoid the cost of tooling a custom screen.*

Screens from Interaction Systems, Kiel, and Touch Technology sense touches to a discrete number of pads or zones, each of which is etched onto the glass with a conductor that's brought out to a dedicated oscillator at the edge of the screen. When a touch changes an oscillator's frequency, controller electronics report the event and the pad number to the computer. **Fig 1** shows the three industry-standard configurations for discrete capacitive touchscreens for CRT monitors. The 32-pad configuration is arranged as 2 columns of 11 rows atop 10 status pads. Kiel's capacitive screens for handheld, liquid-crystal displays feature as many as 75 touch-sensitive areas.

Using a different technique to sense the location of a touch, MicroTouch Systems has developed an analog (padless) capacitive touchscreen. This design places four patterned electrodes with associated oscillators at the corners of the screen; in concert, they apply an ac excitation over the entire display area. When someone touches the screen, the frequencies and amplitudes of all four oscillators change by different amounts. The four changes are then fed to a controller circuit that calculates the contact position with a resolution of 256×256 touch points. (A touch point is the smallest point on a screen that you can define with your fingertip.)

Like their capacitive counterparts, resistive-membrane touchscreens are overlays that clamp or bond snugly to the face of a CRT or flat-panel display. Vendors take different approaches to the technology, but all use some variation of a sandwich principle.

Resistive-membrane screens respond to touch by sensing the contact between a top layer of Mylar and an underlying layer of glass or treated plastic (**Fig 2**). A resistive material on the inside of the sandwich coats both top and bottom layers, and clear-plastic spacer dots a few mils thick separate the two.

Screens from Elographics, Intech Systems, and Tektronix employ a glass bottom sheet. Conductive strips on all four edges of the display apply a voltage across the bottom sheet—first in the X direction, then in the Y direction, at a rate of about 150 times/sec. The top sheet of Mylar senses the voltage drop across the bottom sheet, which is proportional to the position of the touch of any object, conductive or otherwise. Diodes in the electrodes on the periphery of the display decouple the X and Y axes.

In its newer design, Elographics has cut the cost of using diodes by replacing them with a screened, voltage-dividing, thick-film resistive network. A voltage is applied to both corners on the same side of the screen with the other two corners grounded. This operation produces a parabolic—rather than a linear—voltage gradient that's linearized by shaped electrodes, which contact the resistor network at several points along each side.

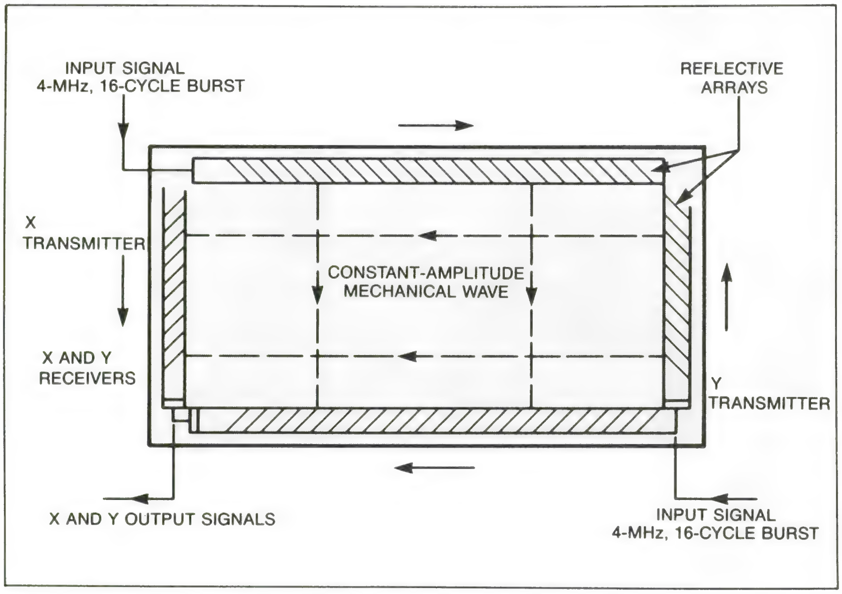
Personal Touch, Sierracin/Transflex, Touch Technology, and TSD Display Products make their sandwiches

A sound approach to touchscreen technology

Zenith has recently announced a type of touchscreen technology that shares many operating principles with ITW Entrex's analog optical system. Using sound rather than light, Zenith's nonoverlay surface-acoustic-wave (SAW) touchscreen supposedly can sense not only the position of a touch with a resolution of 100 touch points per inch, but also the amount of pressure applied with as many as 16 levels of discrimination.

SAW touchscreen technology uses two inexpensive ceramic wafers of piezoelectric material to generate an invisible and inaudible mechanical wavefront on the surface of a screen. Four reflective arrays spatially sample the wavefront and redirect it along multiple parallel paths. The receiving array opposite each transmitter combines the individual wavefronts into a continuous return wave, and the horizontal and vertical arrays are alternately scanned over time. When the screen is touched at a particular location, the wave is attenuated at a corresponding point in time by an amount proportional to the pressure of the touch.

TSD Display Products abandoned SAW technology years ago for reasons of cost, size, and difficulties in retrofitting it to existing displays. Now, however, TSD says that the technology, which Zenith is touting as a cheaper three-dimensional alternative to overlay and optical systems, may be appropriate for new designs.



In a nonoverlay SAW touchscreen, *four reflective arrays sample the wavefront and redirect it along multiple parallel paths. When you touch the screen, the wave is attentuated corresponding to an amount proportional to the pressure of your touch.*

Like their capacitive counterparts, resistive-membrane touchscreens are overlays that bond or clamp to the face of a CRT.

out of plastic materials and sense the position of a touch differently. First a voltage is applied to the top sheet in the orthogonal direction, and the bottom sheet serves as a probe.

Sierracin/Transflex and Touch Technology also build cheaper, discrete resistive-membrane touchscreens, as do Epson America, Fluke, Sharp, and Transparent Devices. These designs also use plastic materials for both halves of the sandwich, but both sheets have discrete rows etched in opposite directions. When the top layer is touched, it deforms to meet the bottom layer; together, the pair acts as a discrete switch whose closure can be sensed as the rows and columns are scanned by the controller. This lower-resolution design eliminates the need to produce and maintain stable linear coatings on the plastic surface, as is required by analog screens.

Optics: Making light work

The third type of touchscreen, variously called optical, LED, or infrared, differs most significantly from the capacitive and resistive-membrane types in that it has no overlay. Optical touchscreen kits contain a frame sized for a particular monitor or flat-panel display, plus controller electronics.

Autech Measurement Systems, Carroll Touch, Electro Mechanical Systems, and Sharp Electronics build screens that tuck dozens of infrared LEDs inside adjacent horizontal and vertical edges of the frame. The inside edges of the frame are made of infrared-transparent material. The light sources are aimed at an equal number of photodetectors located across the display area, under the other two frame edges. This configuration creates an invisible array of dozens of light beams an inch or so above the screen. When a person touches the screen, two beams are interrupted, and one of a discrete number of pads is identified.

Optical touchscreens from ITW Entrex also project an invisible plane of light just above the display, but in a totally different way. Their analog design **(Fig 3)** mounts a single LED on a motor mounted under one corner of the screen. The motor continuously sweeps the LED beam across a 90° arc that corresponds to the display area. Through the joint action of a mirror and a retroreflective material at two sides of the frame, the beam is bounced back from two directions to a photodetector adjacent to the light source.

When the screen is touched, beams from exactly two angles are interrupted. Controller electronics determine the location of the touch by triangulation. This design represents a classic tradeoff: the unreliability of the electromechanical motor for the lower parts count

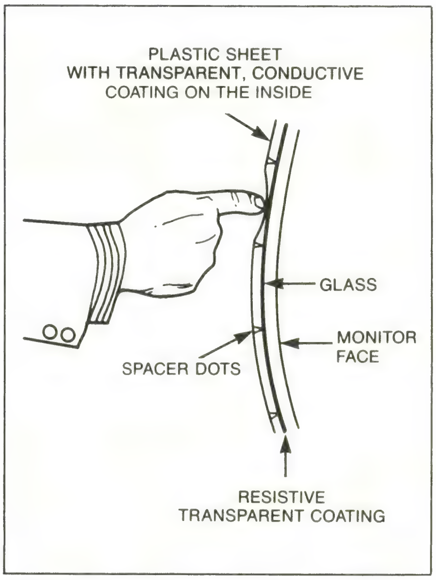


Fig 2—Resistive-membrane screens have a bottom layer of glass *or plastic and a top layer of Mylar; facing sides are coated with a transparent resistive material. Elographics' glass-bottomed screen, for example, has a coating just 1 mil thick.*

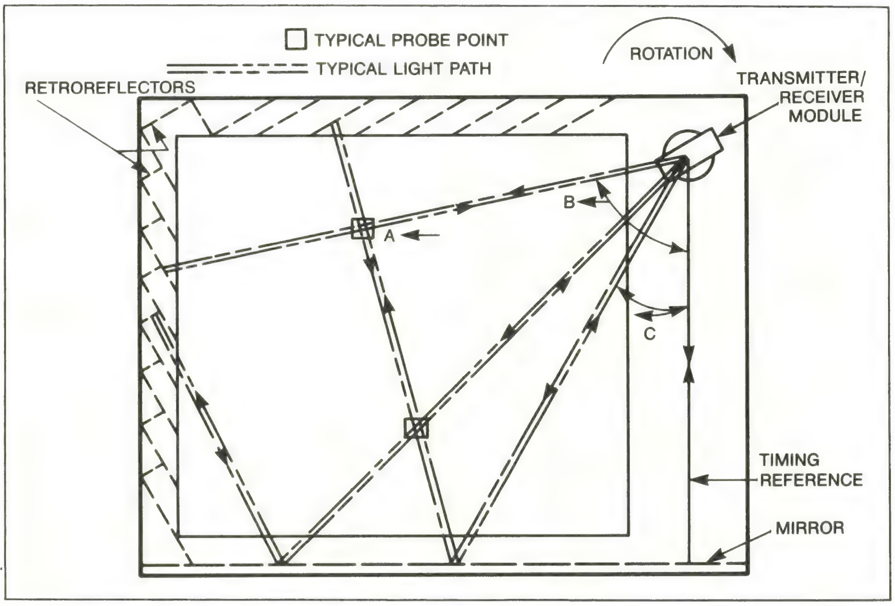


Fig 3—When you touch ITW Entrex's optical screen at point A, *light reaching the detector is blocked at two angles, B and C. The combined action of a mirror at the bottom of the screen and retroreflectors, which reflect light directly back upon itself on the top and left sides, make this operation possible. A microprocessor determines the position of point A by triangulation.*

and cost of fewer LEDs and detectors plus the finer resolution of analog sensing. An upcoming version of this design replaces the motor with a solid-state rotational device but at an increased cost of 20%.

As you might expect, each of the three major touchscreen technologies has inherent performance advantages and disadvantages, especially when compared to the other two **(Table 1).** You shouldn't necessarily rule out a technology simply because it has one characteristic that appears to be inferior to that of another technology. Suitability to the application should be your primary consideration, and you should avoid design overkill.

Resolution: Resistive versions dominate

All vendors agree that analog resistive-membrane screens offer the highest resolution, with possible resolution as great as 4000×4000 touch points. The resolution of screens with two plastic sheets may degrade as coatings wear, however.

Next come the capacitive types; their resolution is 100×100 points typ, 256×256 points max. ITW Entrex's single-source optical design also manages to compete with the capacitive touchscreens: Its resolution spec is 100×80 points max. This number may decrease, however, the farther you get from the light source.

Early capacitive touchscreens were known to suffer from reduced resolution at the sides of the screen and in the corners because of nonlinearities. Nowadays, effective resolution also depends on the variable capacitive loading of the operator. As an extreme case, consider the capacitive swing that might result if a sneaker-clad operator suddenly reached over and touched a metal file cabinet. Capacitive loading effects are handled today by controller firmware, included as part of the controller electronics.

Further down in the resolution standings are all the discrete screens, with their limited number of touch pads. Optical touchscreens also have low resolution. Further, optical systems are singled out for criticism because boosts in their resolution require the addition of expensive LEDs.

Higher resolution is unquestionably desirable in graphics-intensive applications, but you'll find it difficult to ascertain just how much resolution is enough. Touch resolution should be adequate to handle an application's densest menu, taking into account the inherently low resolution of the human finger. Controllers can compensate for a finger overlap of two pads by averaging the position of a finger to a single touch point. At fine levels, however, monitor nonlinearity, which can be as much as 3%, becomes the dominant factor.

Clarity, largely a measure of touchscreen transparency, is arguably more important in graphics-intensive applications than is resolution because a touchscreen's clarity affects the viewing of an entire display, not just the menus. By turning up the brightness control, you might compensate for a touchscreen's low transparen-

TABLE 1—TOUCHSCREEN-TECHNOLOGY TRADEOFFS

	CAPACITIVE SCREEN		RESISTIVE-MEMBRANE SCREEN		OPTICAL SCREEN	
PARAMETER	ANALOG	DISCRETE	ANALOG	DISCRETE	MATRIX	SINGLE-SOURCE
RESOLUTION (NUMBER OF TOUCH POINTS)	100×100 TYP, 256×256 MAX	32 TYP, 100 MAX	1000×1000 TYP, 4000×4000 MAX	8×10 TYP	25×40 TYP, 64×64 MAX	100×80 MAX
CLARITY	85 TO 90%		50% TYP, 80% MAX		100%	
PARALLAX EFFECTS	NONE		NONE		WORST AT EDGES, IN CORNERS	
DURABILITY PROBLEMS	COATING STABILITY		SCRATCHES, COATING WEAR		NONE	MOTOR BURNOUT
ENVIRONMENTAL SENSITIVITIES	TEMPERATURE, HUMIDITY		HUMIDITY		LOW TEMPERATURE, VIBRATION, AMBIENT LIGHT	
EASE-OF-USE PROBLEMS	REQUIRES CONDUCTIVE STYLUS		SLOW TO RESPOND	NONE	SUBJECT TO NONCONTACT TRIGGERING	
INSTALLATION/ MAINTENANCE PROBLEMS	NONE		NONE		ALIGNMENT	MOTOR MAINTENANCE
COST	LESS THAN $1000*		$500 TO $1500*		$500 TO $1500	

*DISCRETE VERSIONS TYPICALLY COST LESS THAN ANALOG ONES.

Touchscreen resolution should be adequate to handle an application's densest menu and take into account the low resolution of the human finger.

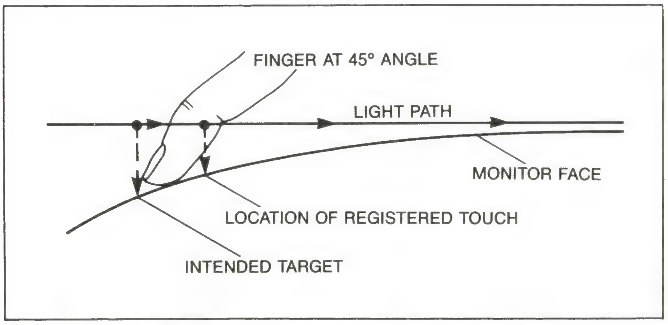


Fig 4—When optical touchscreens are used with curved displays, *parallax can cause operators to miss their targets by as much as an inch. The effect is most pronounced at the edges of the screen, where the distance between the plane of light beams and the surface of the monitor is greatest.*

cy, but doing so might shorten the life of the monitor.

Clarity is clearly highest—100%—for optical touchscreens because such touchscreens don't cover the display with an overlay. Capacitive types usually spec clarity at 85 to 90%. On some discrete capacitive screens, the etched lines are visible.

Resistive-membrane screens typically specify clarity at 50%, but some newer designs claim transparency as high as 80%. Resistive types are prone to glare, which is why some units use a polymer paint on their top surface. Others have gold-tinted Mylar coatings, which tend to give the display a yellow tint. In addition, the use of plastic and spacer dots might make images fuzzy.

Parallax—the apparent change in the position of an object resulting from the change in direction from which it is viewed—is peculiar to optical touchscreens used with monitors. Because light beams can't bend **(Fig 4)**, an optical system must project its invisible grid high enough above the sides, top, and bottom of the monitor to clear the monitor's highest point, in the center of the screen. At the edges, the beam may be as much as an inch and a half above the screen. Some vendors have tried to lower the LED-detector pairs near the edges closer to the monitor face, but this approach reduces parallax effects by no more than 50%.

Optical-touchscreen vendors note that parallax problems are compounded because many menu writers like to position items along the sides of the display where parallax is worst. However, vendors generally dismiss parallax attacks by calling such effects tolerable for most applications. After all, a 19-in. CRT has ⅜-in. parallax at its corners, plus the uniform ¼ in. contributed by its phosphor.

Durability, a measure of a touchscreen's reliability, is difficult to quantify. Usually, though, touchscreen vendors specify durability as a failure rate: MTBF is usually quoted in the 30,000- to 40,000-hour range. Vendors generally agree that capacitive and optical touchscreens last the longest because they have top layers of glass that can only be scratched by a sharp instrument. The stability of the indium tin oxide coating used on capacitive screens raises doubts, though; several vendors are developing alternative coatings like gold and tin antimony. The top plastic layer of resistive-membrane screens, on the other hand, is easier to scratch by accident. Coatings on this top layer have been known to come loose with wear, and the plastic layer itself is certainly more prone to warping than glass.

Durability and reliability are naturally most important in military applications, sensitive or not. Generally, defense contractors seem to favor optical touchscreens because resistive-membrane screens can be scratched and capacitive screens can't respond to the gloved hands of military personnel. At the same time, the edict to avoid custom products in favor of cheaper, off-the-shelf components weakens the case for more costly optical touchscreens.

Different environments, different screens

Touchscreens are showing up in environments ranging from operating rooms to factory floors. Military gear, as usual, commands the most stringent environmental requirements. Computer screens on an aircraft, for example, must be able to work under rapidly changing ambient-light conditions, at extreme temperatures, and in the presence of severe levels of shock and vibration. Low temperatures are a particular problem for optical touchscreens because of resulting reductions in the gain and sensitivity of the photodetector transistors.

Another harsh environment in which touchscreens are suitable but have the potential for troublesome operation is in the automobile. Even in the passenger compartment, where a touchscreen might simplify the operation of a trip computer, for example, extreme temperatures and lots of shock and vibration can wreak havoc with any sensitive device. However, a resistive-membrane screen from Sierracin/Transflex has been part of the Buick Riviera's graphic control center for three model-years. Although some skeptics consider this application an anomaly, other vendors are ruggedizing their screens and electronics service for cars, trucks, and factory-floor control systems.

Generally, optical systems are thought to be less

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Parallax problems are compounded by the fact that many menu writers like to position items along the sides of a display.

prone to environmental effects than overlay-type touchscreens, despite their problems relating to low temperatures and even though excessive vibration can cause LED-detector alignment problems. Capacitive screens are sensitive to temperature and humidity, whereas resistive-membrane types are prone to trapping condensation between their two Mylar layers.

All three types are affected to some degree by smoke and dust, but optical screens come under the most criticism for being sensitive to the accidental breaking of their beams by errant flies and shirtsleeves. Mike Lazarevich of Electro Mechanical Systems suggests that it's possible to equip touchscreens with an object-recognition circuit that could distinguish between, say, a moth and a finger by analyzing their different spatial profiles over time.

Ease of use may determine whether touchscreen technology will sink or swim in the turbulent waters of the information revolution. Vendors of overlay touchscreens claim that optical systems' ability to register touch without actual screen contact can be disconcerting to novice computer users. Those in the optical camp counter that capacitive screens' requirement of a conductive stylus is too restrictive, that resistive screens' sensitivity to pressure reduces response time, and that the use of spacer dots can cause bounces and skips on lines drawn by a finger.

Ease of use also relates to installation and maintenance. All three types of touchscreens require the same sort of installation, so tradeoffs between technologies are minimal. The sole exception is Personal Touch's resistive-membrane screen, which attaches to monitors by Velcro strips. Thus, you can remove it and use it on a desktop or your lap as an 8½×11-in. digitizing tablet.

Regarding maintenance, some single out the rotational-LED optical system, with its under-the-bezel motor, as difficult to service. Others charge that optical screens go out of alignment each time you remove the monitor. In their own defense, optical-screen vendors point out that alignment tolerances aren't as tight as you might think: LEDs typically emit a cone of light that is 30 or 40 degrees across.

Prices of touchscreens for CRT monitors have progressively decreased over the last decade. Screens that cost more than $1000 just a few years ago now sell for roughly half that. Cost-reduction efforts have almost universally centered on controller electronics, which typically constitute about one-third the total cost of a touchscreen kit. Most suppliers are turning to custom chips, gate arrays, and highly integrated microsystem

For more information . . .

For more information on the touchscreens described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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7060 Huntley Rd
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(614) 888-9924
Circle No 626

Carroll Touch (O)
2800 Oakmont Dr
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(512) 244-3500
Circle No 627

Electro Mechanical Systems (O)
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Elographics Inc (R)
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(615) 482-4100
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John Fluke Manufacturing Co Inc (R)
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(800) 426-0361
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Circle No 632

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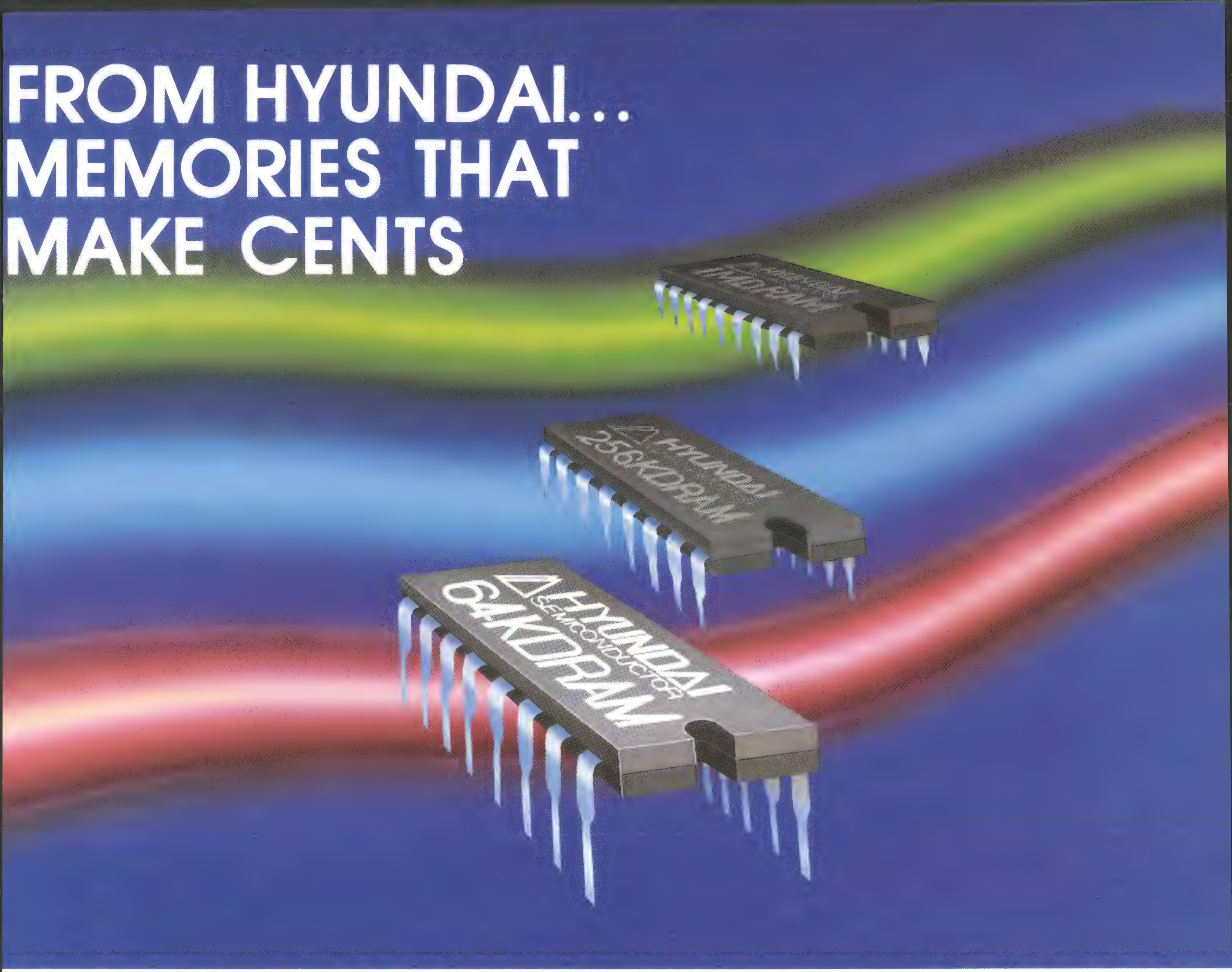
Legend:
C=Capacitive
R=Resistive
O=Optical
S=Surface-acoustic-wave
F=Flat panel only



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		HY61C67/L	16K x 1 BIT	35,45,55	+5V	50mA	100uA	20
		HY61C68/L	4K x 4 BIT	35,45,55	+5V	60mA	100uA	20
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☐	64K SRAM	HY6264	8K x 8 BIT	45,55,70	+5V	100mA	10mA	28
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☐	256K DRAM	HY51C256L	256K x 1 BIT	100,120,150,200	+5V	55mA	2mA	16
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CIRCLE NO 124

Cost-reduction efforts have almost universally centered on controller electronics, which typically contribute to one-third the cost of a kit.

components to reduce the parts count of controller cards from nearly 100 to 25 or so.

Single-unit prices for touchscreen kits range from a few hundred dollars to more than a thousand dollars for popular CRT models; custom kits for less-popular monitors are available for similar prices, plus a tooling charge of $10,000 to $100,000. Most vendors also sell inexpensive versions of the touchscreens for LCD flat-panel displays. Some also support plasma and electroluminescent units.

System builders, however, continue to demand lower prices. Electro Mechanical Systems theorizes that OEMs won't be satisfied with the price of a touchscreen until it's no more than 10% of the price of the monitor to which it is attached. Considering that dumb terminals now sell in the $400 range, touchscreen vendors have a long way to go.

Analog resistive-membrane touchscreens have superior resolution but generally cost about the same as optical screens, which range in unit price from $500 to $800 for a 9-in. frame to $900 to $1500 for a 19-in. model. Resistive-screen controllers, simple and amenable to cost reduction, usually add about $200 to $300 to the total price of the kit. Discrete resistive-membrane screens are slightly less expensive. The lowest priced resistive-membrane touchscreen ($200) is manufactured offshore by Personal Touch. Designed for displays with 10- to 15-in. diagonal measurements, the unit specs a resolution of 250×250 touch points. Capacitive screens, which use simple sensors and complex controllers, generally cost less than $1000. This price, however, might not include the controller.

Touchscreens for flat-panel displays, a market that hasn't yet been adequately pursued by touchscreen vendors, are nonetheless considerably cheaper than those for CRT monitors. For example, Epson America sells discrete and analog versions of a 280×180-mm (11×7-in.) resistive-membrane screen for about $100 (OEM qty). These glass-and-plastic units are just 1.4 mm thick and spec clarity at 70%, resolution at 1.3 mm (0.05 in.), and durability at 1 million touches. Kiel's touchscreen for 8-row×40-column LCDs sells for $250 and can be configured with a matrix of 10×4 to 10×16 touch pads.

Everyone seems to concur that there is a lower limit to optical-touchscreen prices because of their use of relatively expensive LEDs. Carroll Touch and Electro Mechanical Systems, the two largest optical-screen suppliers, are attacking this problem by developing patented low-light circuits that can respond to millivolt signals produced by photodetectors. This approach will allow them to use less-powerful, cheaper LEDs. Electro Mechanical Systems even boasts that if it got an order today for 10,000 touchscreens, it could price them at just $98 each.

With touchscreen performance up and costs down, vendors and OEMs are turning their attention to that old nemesis of the computer business: software development. You can't just tack a touchscreen onto a display and expect it to work with off-the-shelf applications software.

OEMs of general-purpose systems face a chicken-and-egg problem with regard to touchscreen software. Big software houses are understandably reluctant to develop touch-activated versions of their best sellers until it's clear that a new touchscreen-equipped system has a good chance for success. That success won't happen, however, unless end users can see how touch can improve their favorite programs.

In business computing, touch-sensitive systems and software seem most appropriate for users such as stockbrokers, whose passion for productivity is legend. Touch-activated versions of complex packages like Lotus 1-2-3 and Wordstar are also growing in popularity among novice users because they eliminate the need to memorize or look up lengthy keyboard-entry codes, which in turn allow access to arcane subroutines. Personal Touch, aiming squarely at the end-user market, includes five touch-compatible applications packages with its $200, user-installed Apple II computers and IBM PC-compatibles: a simple word processor, a graphics creator, an everyday spreadsheet, a checkers package, and a puzzle.

For OEMs of special-purpose computers like process-control systems, the burden of software development is theirs alone. Most touchscreen vendors now offer software-development tool kits containing drivers, editors, subroutine libraries, and the like. To maximize the utility of a touchscreen, the applications code that supports it must reflect attention to both human factors and the screen's technical characteristics. For example, menus for low-resolution touchscreens should be dense enough to speed up a complex procedure, yet not so dense that they risk the accidental selection of an incorrect choice. **EDN**

John Javetski is a free-lance writer.

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CIRCLE NO 125

Designer's Guide to VME Bus Control—Part 2

FPCs and PLDs implement VME Bus slave controllers

By using fuse-programmable controllers (FPCs) and PLDs, you can implement VME Bus control in your computer system with a minimum of hardware. Part 1 (October 2, pg 187) of this 2-part series described the bus-arbitration process and control functions and showed how to implement the VME Bus data-transfer protocol in an FPC. This second and final part describes the implementation of similar controllers for slave modules and interrupt handlers, and it provides tools for programming the FPC.

Arthur Khu, *Advanced Micro Devices*

When you offload a system's bus-control functions from the CPU to a hardware bus controller, you considerably reduce the time these functions require, thereby improving the data-transfer rate over the bus. You can substantially reduce the cost and chip count of such a bus controller by implementing the bus-control logic in VLSI devices such as fuse-programmable controllers (FPCs) and programmable logic devices (PLDs).

The VME Bus protocol requires that all data transfers over the bus be initiated by a master module. Your system can include several master modules, such as CPUs or DMA controllers; a bus-arbiter module arbitrates simultaneous data-transfer requests from two or more masters. No data transfer can take place until the requesting master has been given control of the bus by the bus arbiter.

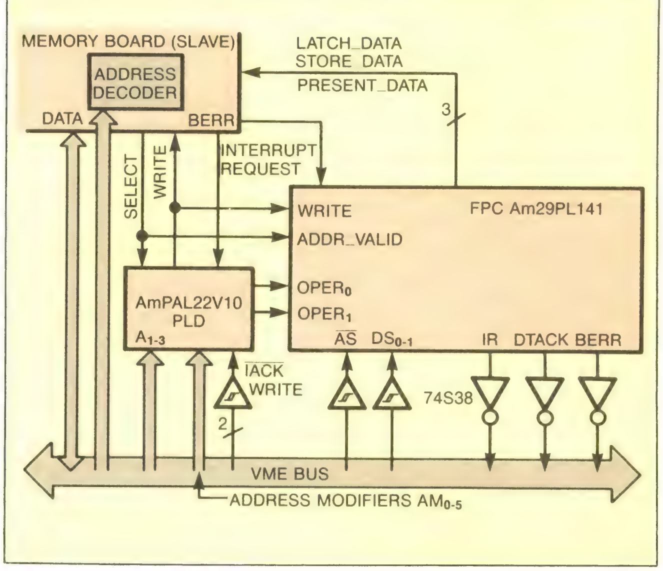


Fig 1—This device controller, *which is implemented with an FPC and a PLD, handles data-transfer and interrupt protocols for a slave device in a VME Bus system.*

Because a slave can't initiate a data transfer, your system must include an interrupt mechanism that allows a slave to request service from a master. You can implement such a mechanism in your system by designing a slave subsystem like the one in **Fig 1.** This slave subsystem comprises a slave module and a slave interrupt controller. The slave interrupt controller, which consists of an Am29PL141 FPC and an AmPAL22V10 PLD, serves as the interface between the slave subsys-

The interrupt controller for a slave device implements the interrupt protocol in hardware.

tem and the VME Bus structure. Once the master has initialized the slave, it can issue commands to the slave. The slave performs these tasks in the background, leaving the master free to continue its own operations. When the slave is ready to return the status or result of a task to the master, it issues an interrupt request.

The VME Bus single-cycle data-transfer protocol defines the interactions between master and slave controllers **(Fig 2)**. When the master drives the address strobe ($\overline{AS}$) low, the slave controller latches the address presented on the bus, and a separate address-decoding unit on the slave board decodes the address. If the address is not valid (ie, if it's not in the range associated with this slave), the slave takes no further action. However, if the address selects this slave subsystem,

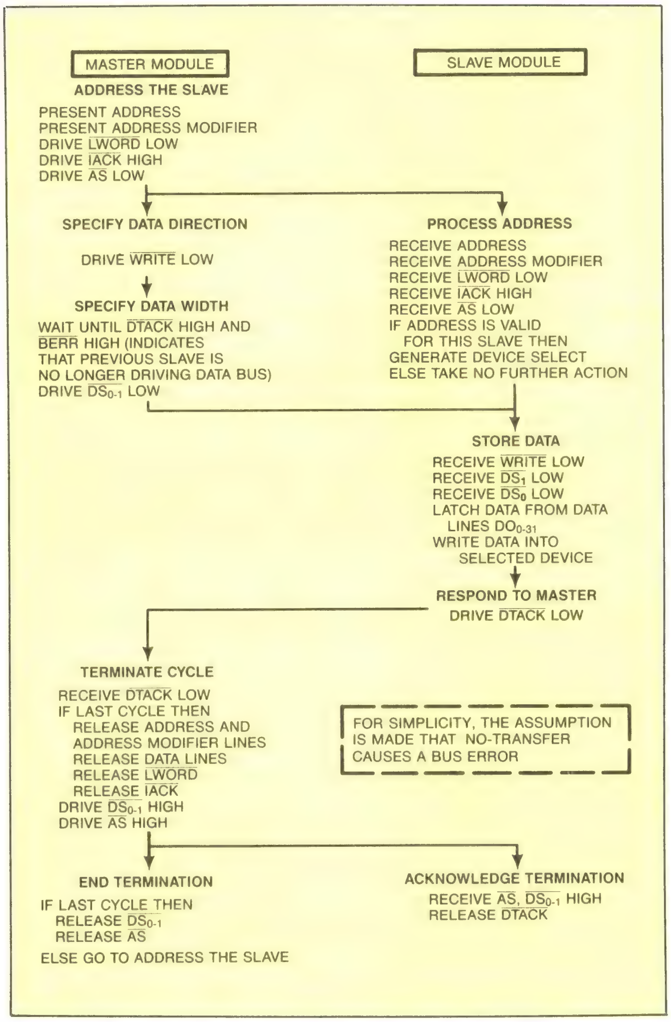
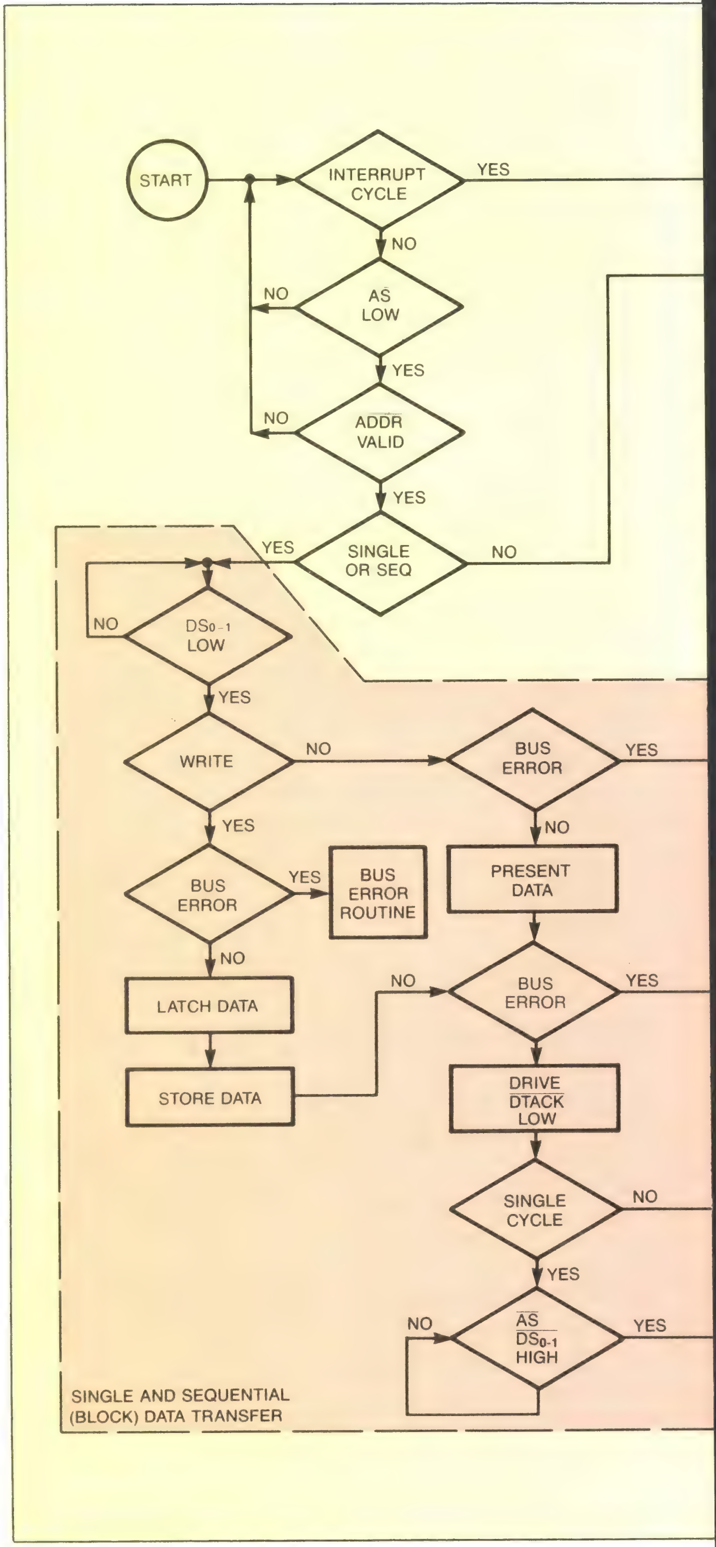


***Fig 2—The slave controller recognizes its own address** and receives a data word from the bus master in this flow diagram for single-cycle transfer.*



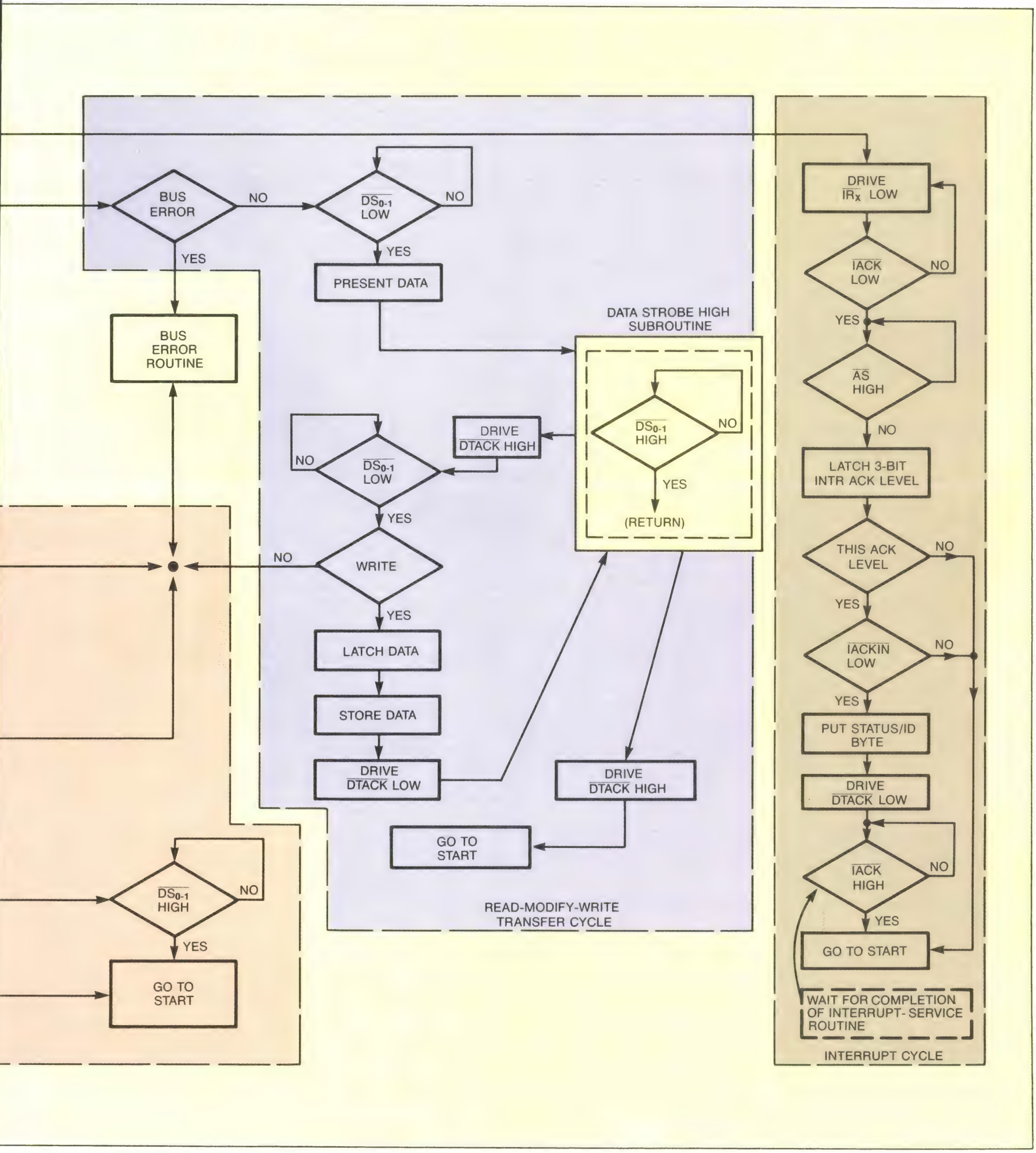

BUS ERROR
NO
$\overline{DS_{0-1}}$ LOW
NO
YES
YES
PRESENT DATA
BUS ERROR ROUTINE
DATA STROBE HIGH SUBROUTINE
DRIVE $\overline{DTACK}$ HIGH
NO
$\overline{DS_{0-1}}$ LOW
YES
$\overline{DS_{0-1}}$ HIGH
NO
YES
(RETURN)
NO
WRITE
YES
LATCH DATA
STORE DATA
DRIVE $\overline{DTACK}$ LOW
DRIVE $\overline{DTACK}$ HIGH
GO TO START
NO
$\overline{DS_{0-1}}$ HIGH
YES
GO TO START
READ-MODIFY-WRITE TRANSFER CYCLE
DRIVE $\overline{IR_X}$ LOW
$\overline{IACK}$ LOW
NO
YES
$\overline{AS}$ HIGH
NO
LATCH 3-BIT INTR ACK LEVEL
THIS ACK LEVEL
NO
YES
$\overline{IACKIN}$ LOW
NO
YES
PUT STATUS/ID BYTE
DRIVE $\overline{DTACK}$ LOW
$\overline{IACK}$ HIGH
NO
YES
GO TO START
WAIT FOR COMPLETION OF INTERRUPT-SERVICE ROUTINE
INTERRUPT CYCLE

Fig 3—This state-machine diagram *for* ***Fig 1's*** *slave controller is derived from the flow diagram in* ***Fig 2****. The state machine has four modes, which handle interrupts as well as single, block, and read-modify-write data transfers.*

The VME Bus protocol requires that all data transfers over the bus be initiated by a master module.

the slave looks for signals from the master that specify whether a read or a write operation should take place. After presenting or storing data, the slave controller drives the data-transfer-acknowledge signal ($\overline{\text{DTACK}}$) low to inform the master of the successful transfer.

From the VME Bus-protocol flow diagrams **(Fig 2)**, you can derive a state diagram **(Fig 3)** for the slave-controller state machines; **Fig 4** shows the resulting timing pattern for the slave controller. You can develop microcode for the slave controller's single-cycle transfer mode from the state diagram and the timing pattern. Use the address-modifier lines ($AM_{0\text{-}5}$) to specify the other three slave operating modes (sequential, or block, transfers; read-modify-write transfers; and interrupt cycle). To recognize these special modes, the slave controllers on each slave board constantly monitor the six address-modifier lines.

When the code presented on the address-modifier lines specifies a block-transfer operation, the master retains control of the bus throughout the operation by holding $\overline{\text{AS}}$ and $\overline{\text{BBSY}}$ low. For a block transfer, bus arbitration takes place only once, before the start of the operation; for single-cycle transfers, bus arbitration takes place before the transfer of each word. A block transfer, therefore, takes less time than does the corresponding number of single-word transfers.

At the start of a block-transfer operation, all the slaves load the address presented on the bus into their address counters and decoders, but only the slave whose memory range encompasses the decoded address responds to the data-transfer request. As each word transfer is completed, all the slaves increment (or decrement) their address counters and decode the new address. This procedure is necessary because the memory block being transferred may reside on more than one slave memory board.

In the slave subsystem in **Fig 1,** the PLD decodes control signals from the bus and slave board and sends two signals, $OPER_0$ and $OPER_1$, to the slave's FPC. The FPC decodes these two signals, along with inputs from

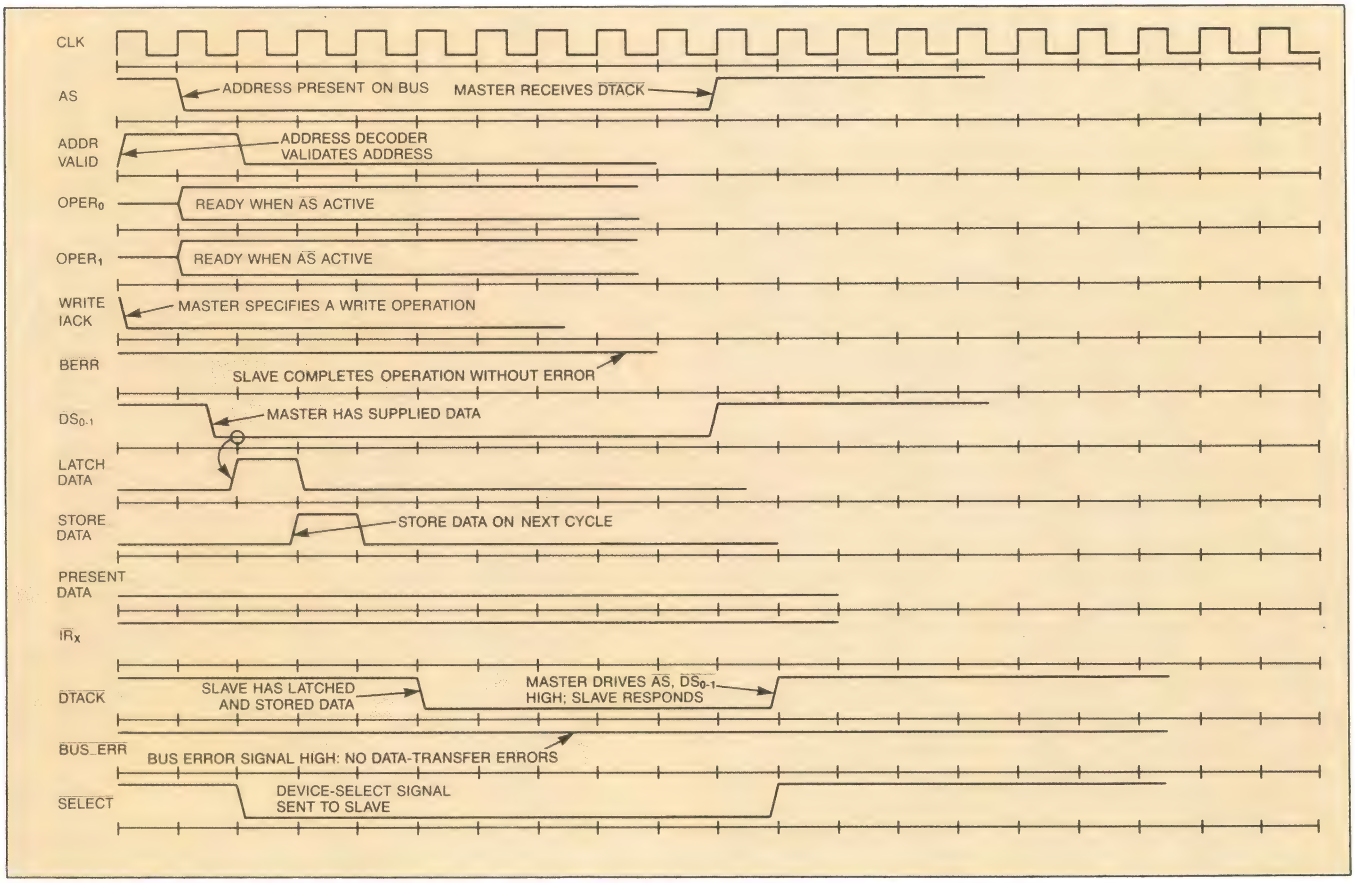

CLK
AS
ADDRESS PRESENT ON BUS
MASTER RECEIVES DTACK
ADDR VALID
ADDRESS DECODER VALIDATES ADDRESS
OPER0
READY WHEN AS ACTIVE
OPER1
READY WHEN AS ACTIVE
WRITE IACK
MASTER SPECIFIES A WRITE OPERATION
BERR
SLAVE COMPLETES OPERATION WITHOUT ERROR
DS0-1
MASTER HAS SUPPLIED DATA
LATCH DATA
STORE DATA
STORE DATA ON NEXT CYCLE
PRESENT DATA
IRx
DTACK
SLAVE HAS LATCHED AND STORED DATA
MASTER DRIVES AS, DS0-1 HIGH; SLAVE RESPONDS
BUS_ERR
BUS ERROR SIGNAL HIGH: NO DATA-TRANSFER ERRORS
SELECT
DEVICE-SELECT SIGNAL SENT TO SLAVE

Fig 4—You'll need to generate a timing diagram *for each of the slave controller's operating modes. This diagram shows the timing for a single-cycle data transfer.*

the slave, bus, and address-decoding units on the slave board, to determine which of the four possible slave operating modes to execute. The four modes, which are designated by binary codes, specify the following operations:

- (00) Perform a single-cycle transfer
- (01) Perform a sequential-cycle transfer
- (10) Perform a read-modify-write cycle
- (11) Perform an interrupt cycle.

If OPER_0 and OPER_1 are both high, the FPC operates as an interrupter by branching to an interrupt subroutine **(Fig 3).**

When the slave requests an interrupt, the FPC generates an interrupt-request signal and waits for the interrupt-acknowledge signal ($\overline{\text{IACK}}$) and daisy-chain signal ($\overline{\text{IACKIN}}$). When the data strobes become active, the PLD reads a 3-bit value from the address bus ($A_{1\text{-}3}$); this value indicates which interrupt-request line was acknowledged. The PLD decodes these three bits to determine whether their value matches its own request level; if it finds no match, no further action occurs. If it does find a match, however, the PLD routes a valid signal to the FPC, indicating that the interrupt handler has acknowledged the slave's interrupt request. The FPC then signals the slave board to put its status or identification byte on the data bus for the interrupt handler to use as an interrupt vector. The slave FPC waits in a loop until the interrupt handler drives the $\overline{\text{IACK}}$ signal high to signify that interrupt service is complete.

Besides containing master, slave, and bus-arbiter modules, a VME Bus system usually has an interrupt-handler module that handles external I/O or special system events (time-out or overflow errors, for example). You can reduce the logic complexity of the interrupt-handler module in your system by offloading some of the initial interrupt-recognition tasks to an interrupt-handling preprocessor (IHP). You can use a PLD as the IHP, programming it to preprocess interrupt requests, obtain control of the bus, and handle hand-

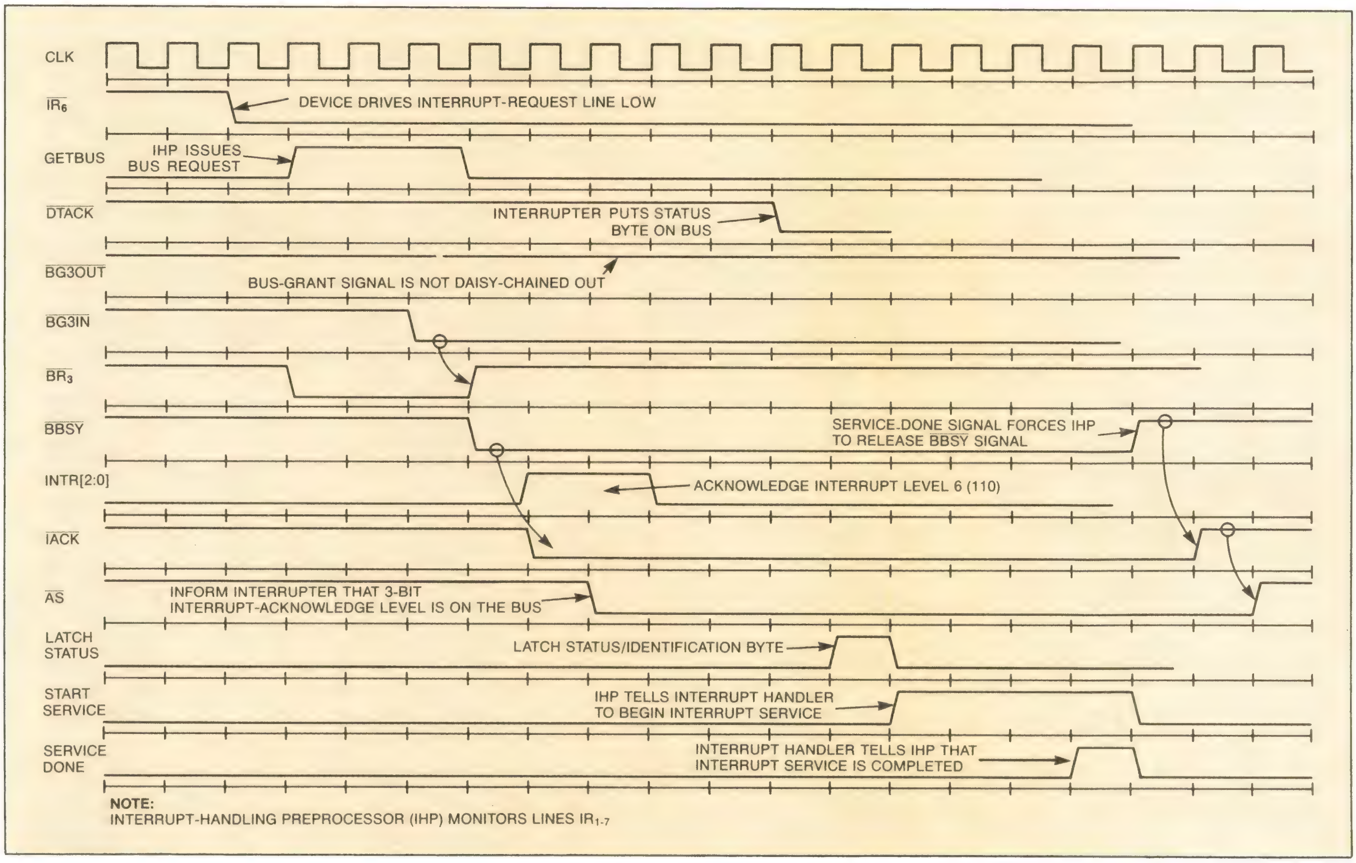

CLK
$\overline{IR_6}$
DEVICE DRIVES INTERRUPT-REQUEST LINE LOW
GETBUS
IHP ISSUES BUS REQUEST
$\overline{DTACK}$
INTERRUPTER PUTS STATUS BYTE ON BUS
$\overline{BG3OUT}$
BUS-GRANT SIGNAL IS NOT DAISY-CHAINED OUT
$\overline{BG3IN}$
$\overline{BR_3}$
$\overline{BBSY}$
SERVICE-DONE SIGNAL FORCES IHP TO RELEASE $\overline{BBSY}$ SIGNAL
INTR[2:0]
ACKNOWLEDGE INTERRUPT LEVEL 6 (110)
$\overline{IACK}$
$\overline{AS}$
INFORM INTERRUPTER THAT 3-BIT INTERRUPT-ACKNOWLEDGE LEVEL IS ON THE BUS
LATCH STATUS
LATCH STATUS/IDENTIFICATION BYTE
START SERVICE
IHP TELLS INTERRUPT HANDLER TO BEGIN INTERRUPT SERVICE
SERVICE DONE
INTERRUPT HANDLER TELLS IHP THAT INTERRUPT SERVICE IS COMPLETED
NOTE:
INTERRUPT-HANDLING PREPROCESSOR (IHP) MONITORS LINES $IR_{1\text{-}7}$

Fig 5—The interrupt-handling preprocessor *monitors the seven VME Bus interrupt-request lines ($\overline{IR}_{1\text{-}7}$), identifies the interrupting device, and tells the interrupt handler when to begin servicing the interrupt. This timing diagram shows the signal states that exist before and during the transfer of the identification and status bytes from the slave-interrupt subsystem to the interrupt handler.*

When the slave module is in block-transfer mode, bus arbitration takes place only once before the start of the operation.

shaking signals (such as interrupt-acknowledge signals). Only when the IHP latches the interrupt vector will control pass to the interrupt-handler module.

To define interrupt-request processing, bus acquisition, and the interrupt vector's transfer phase, you'll have to use logic equations written in high-level Boolean notation. In the design in **Fig 1,** the PLD monitors seven interrupt-request lines and four data-transfer control inputs, and it sends 10 control signals to the interrupt handler and the VME Bus drivers. The PLD monitors all interrupt-request lines according to the following logic equation:

```
IF (IR1 + IR2 + IR3 + IR4 + IR5 +              (1)
  IR6 + IR7) THEN
BR3 : = 1 ;
        "THIS INTERRUPT HANDLER USES"
        "THE BR3 REQUEST LINE"
```

If any interrupt-request line is active, the PLD asserts $\overline{\text{BR3}}$ to initiate the bus-acquisition phase.

The next step is to wait for the bus-grant-in signal. Only when $\overline{\text{BGIN3}}$ is active will $\overline{\text{BBSY}}$ be active. The logical expression of this condition is given in the following equations:

```
IF (BR3*/BG3IN) THEN                                   (2)
        BR3 : = 1 ;

IF (BR3*BG3IN + BBSY*/SERVICE_DONE) THEN (3)
       BBSY : =  1 ;
```

Eq 2 continually asserts $\overline{\text{BR3}}$ as long as $\overline{\text{BG3IN}}$ is not active; **Eq 3** asserts $\overline{\text{BBSY}}$ only when request line $\overline{\text{BR3}}$ and $\overline{\text{BG3IN}}$ are active, or if service is not complete after the IHP asserts $\overline{\text{BBSY}}$.

When the IHP is the bus master, it puts the 3-bit

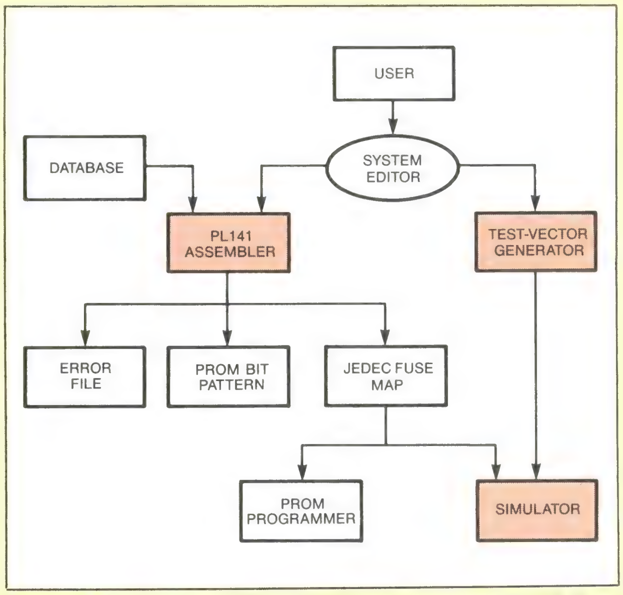
Development tools help you program FPCs

The Am29PL141 is a single-chip fuse-programmable controller (FPC) that can implement state machines and distributed control functions. You can express and functionally verify these state machines and functions by using three FPC-development tools provided by the manufacturer: an assembler, a test-vector generator, and a simulator. These development tools, which are written in C, run on an IBM PC or compatible computer under MS-DOS. Source code for the programs is available, so you can port the software to other systems.

The FPC has a control store that's resident in its PROM; the store is 64 words long and 32 bits wide. Instructions such as jumps, loops, and subroutine calls in the PROM control store are conditionally executed by the 20-MHz internal sequencer. Each 32-bit instruction is partitioned into the following format:

BITS:	1	5	1	3	6	16
FIELD:	OE	OPCODE	POL	TEST	DATA	OUTPUT

The output field contains the 16 control outputs that the FPC generates when it executes an instruction. The upper eight output bits are controlled by the output enable (OE) bit; they may be high, low, or disabled. The lower eight output bits are always enabled. The op-code field specifies which of the 29 possible instructions the FPC will execute if the condition selected by the test



To program the Am29PL141 FPC to implement VME Bus-control functions, *you can use the assembler, test-vector generator, and simulator provided by the FPC's manufacturer. These development tools, which are written in C, run on an IBM PC or compatible computer under MS-DOS.*

interrupt-line-acknowledge value on the bus and asserts the data strobes. Upon receipt of the $\overline{\mathrm{DTACK}}$ signal from the interrupter, the IHP strobes the status byte from the bus into a register on the interrupt-handler card. The IHP then informs the interrupt handler that a status/identification byte is ready and that the handler should begin servicing the interrupt. The IHP resolves interrupt priorities within a single clock cycle because all interrupt/input signal lines are processed in parallel by the logic array in the PLD. **Listing 1** shows how you'd express the procedure in a logic-description language.

LISTING 1

```
IF  (BBSY) THEN
     BEGIN
(1) IF (IR7) THEN                 "IR7 was active                 "
         INTR[2:0] : = 7 ;        "3-bit value acknowledging
                                   interrupt line 7               "
    IF (/IR7*IR6) THEN            "IR6 active, IR7 inactive       "
         INTR[2:)] : = 6 ;        "acknowledge interrupt line  6"
    IF (/IR7*/IR6*IR5) THEN       "IR5 highest priority           "
         INTR[2:0] : = 5 ;        "interrupt line active          "
                 :
                 :
                 :
(2) IF (/IR7*/IR6*/IR5*/IR4*/IR3*/IR2*IR1) THEN
         INTR[2:0] : = 1 ;        "acknowledge interrupt line  1"
END;
```

As you can see from **Listing 1,** if both the $\overline{\mathrm{IR7}}$ and the $\overline{\mathrm{BBSY}}$ signals are active in section 1, then the 3-bit value generated by the IHP will be binary 111 (decimal 7), regardless of the state of the other interrupt lines. In section 2, if $\overline{\mathrm{IR1}}$ and $\overline{\mathrm{BBSY}}$ are active and the other six control signals are inactive, then the 3-bit output value will be binary 001 (decimal 1). In section 2, $\overline{\mathrm{IR1}}$ is the highest priority line that is active.

The remaining interrupt-preprocessing steps complete the transfer of the interrupt-vector byte; this transfer is described logically in the following

```
IF  (BBSY) THEN                                                   (4)
    BEGIN
    IACK := 1;                   "begin interrupt acknowledge daisy"
(X) IF (DTACK) THEN              "chain; if device sends data      "
      LATCH_STATUS := 1;.        "transfer acknowledge (DTACK)     "
                                 "signal, then latch the status    "

    END:
IF  (IACK) THEN
    AS := 1;                "assert the address strobe signal to inform the
                             interrupter that the interrupt acknowledge
                             level is ready"
```

---

field is true. The polarity bit (POL) determines whether a high input or a low input represents true for the test input selected. You can use the data field as an argument for the op-code field. For example, if you want the FPC to jump (op code 25) to location 34 (22_{HEX}) when the second bit in the test field is high (true), you put the following 32-bit word into the control store (though you'll also have to define the OE bit and the output bits):

```
OE 11001 0 010 100010 OUTPUT
```

The assembler simplifies system design by allowing you to use a high-level language. Instead of specifying the bit patterns shown above, you can write the following section of code:

```
OUTPUT , IF (T2 = 1) THEN
                   GOTO PL (34);
```

The assembler translates this statement into the appropriate bit patterns; when the FPC executes the instruction, it generates the bit pattern defined by the symbol OUTPUT.

Every microinstruction written in assembly language follows this format:

```
< LABEL : > OUTPUT , STATEMENT ;
```

The label field, which is optional, simplifies the writing of subroutine calls and conditional branch instructions, which you can express in IF-THEN-ELSE, WHILE-DO, or COMPARE forms. Once you've written all the instructions with the editor and translated them to executable form with the assembler, you can cause the assembler to generate a JEDEC fuse map.

Before physically programming the PROM control store that you've designed, you can test your design with the help of the test-vector generator and simulator. The test-vector generator produces test vectors, from a user-generated truth table, and converts them into a JEDEC-standard test-vector file that the simulator can use.

The simulator performs two important functions: It verifies the control flow of your design, and it checks the fuse map that the assembler generates. By using the simulator's interactive mode, you can inspect, modify, or preset any of the internal registers in the FPC. The simulator also has single-stepping and break-point features so that you can trace the operation of your design in detail.

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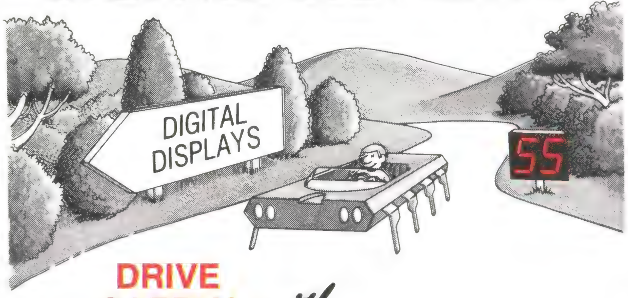

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CIRCLE NO 126

An interrupt-handling preprocessor can off-load some of the initial interrupt-recognition tasks of your system's interrupt-handler module.

Once the assertion of the $\overline{\text{DTACK}}$ signal indicates the successful transfer of the 8-bit status or identification byte, the IHP instructs the interrupt-handler module to begin the interrupt-service routine. This instruction from the IHP is logically defined as follows:

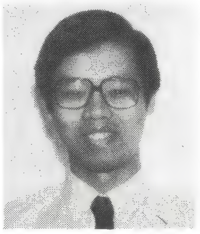
```
IF (BBSY*LATCH_STATUS + BBSY*                    (5)
  START_SERVICE*/SERVICE_DONE) THEN
START_SERVICE : = 1;
```

This definition states that the IHP constantly asserts the START_SERVICE signal until the interrupt handler generates a SERVICE_DONE signal, at which point the IHP drives START_SERVICE low. The logic described above generates the timing diagram shown in **Fig 5.**

Development tools simplify controller design

Development tools provided by FPC and PLD manufacturers simplify the task of programming these devices as VME Bus controllers. Once you've analyzed the bus protocols and converted these into state-machine diagrams, you can write assembly-language programs and high-level logic equations to describe the state machines. The assembler and logic software will then process these programs and equations to fit into the FPC or PLD. For a summary of the programming tools available for the Am29PL141 FPC, see **box,** "Development tools help you program FPCs." **EDN**

Author's biography



Arthur Khu, a product planning engineer for Advanced Micro Devices (Sunnyvale, CA), is responsible for research and definition of advanced programmable-logic-device architectures. He holds a BS in Math/Computer Science and an MS in Computer Science from Santa Clara University. In his spare time, Art enjoys racquetball and astronomy.

Article Interest Quotient (Circle One)
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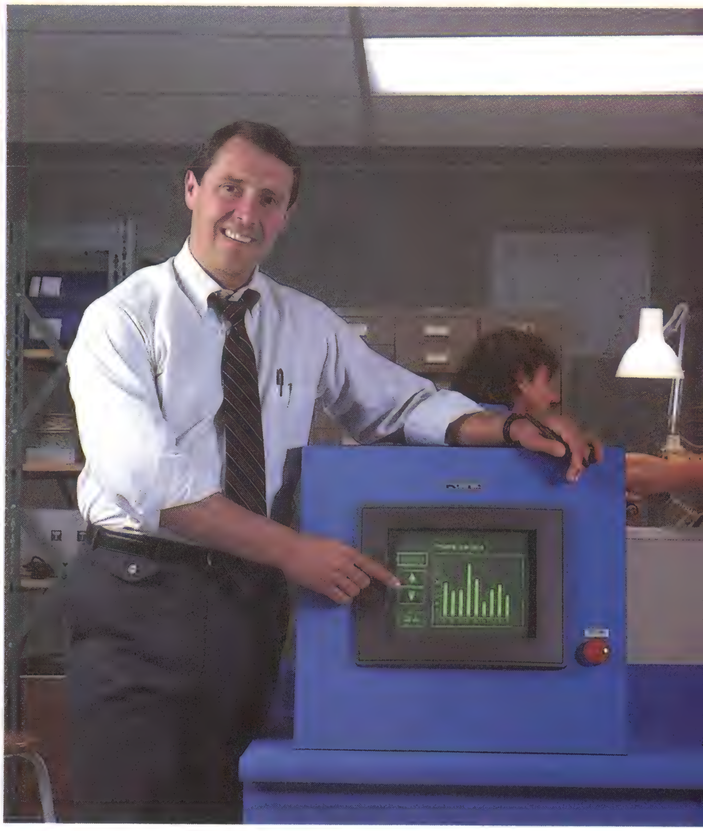

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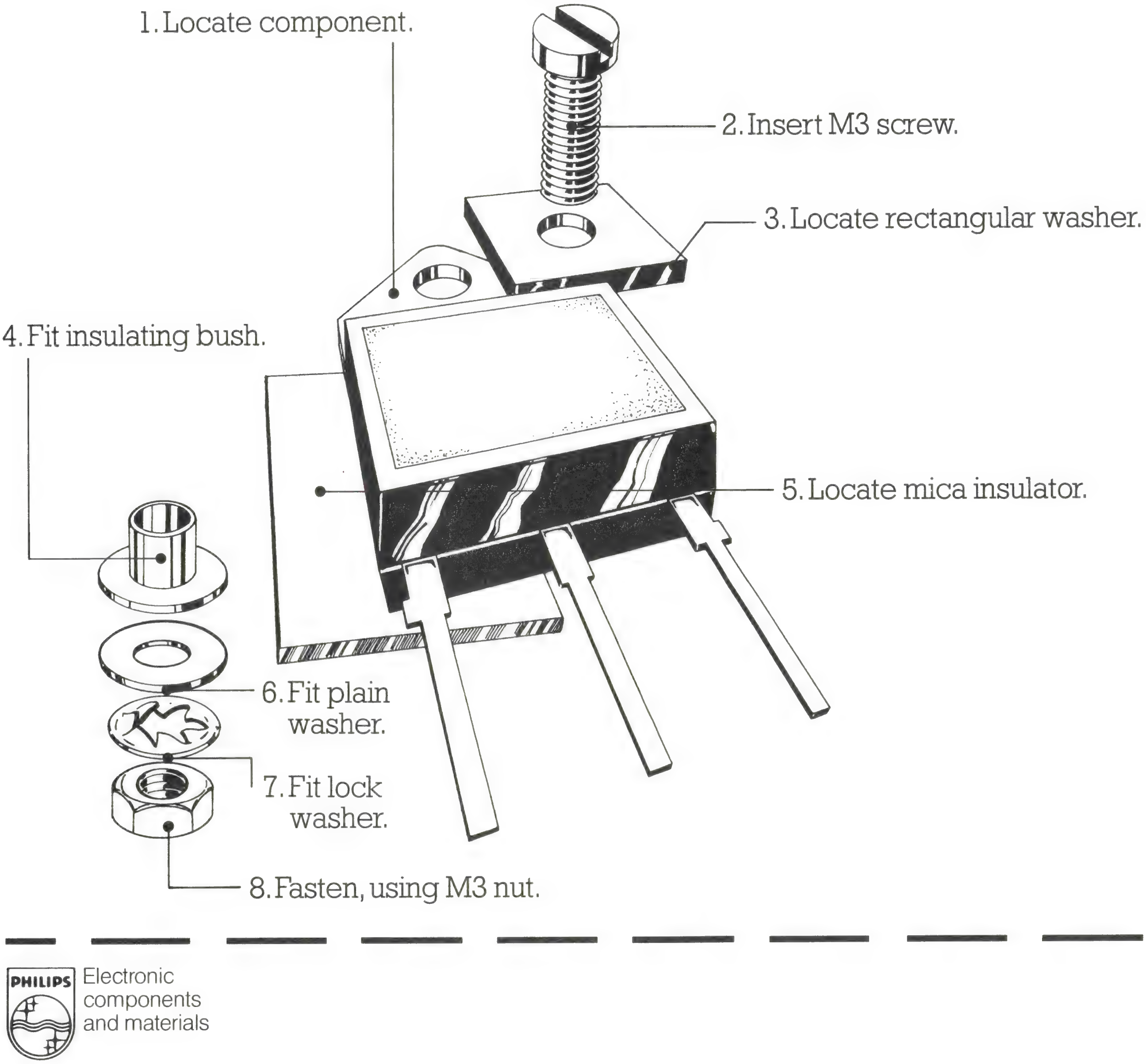

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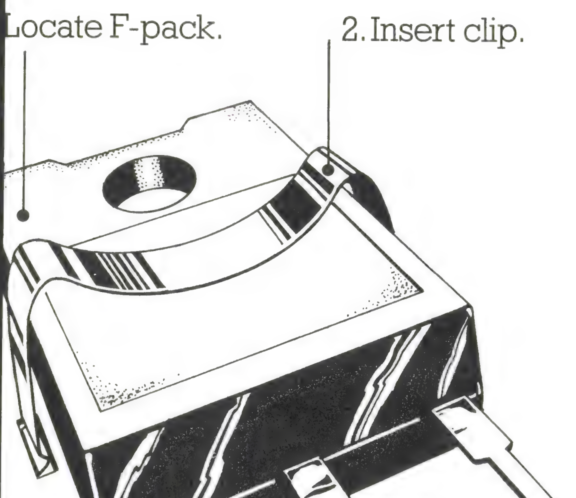

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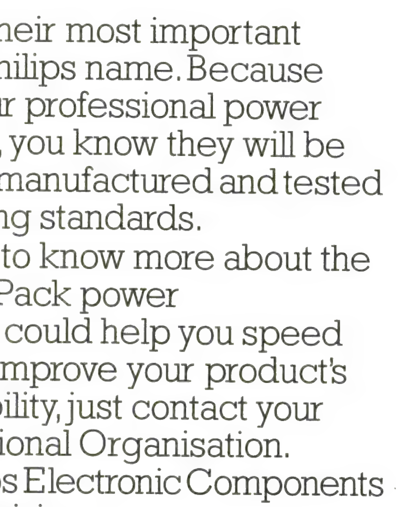

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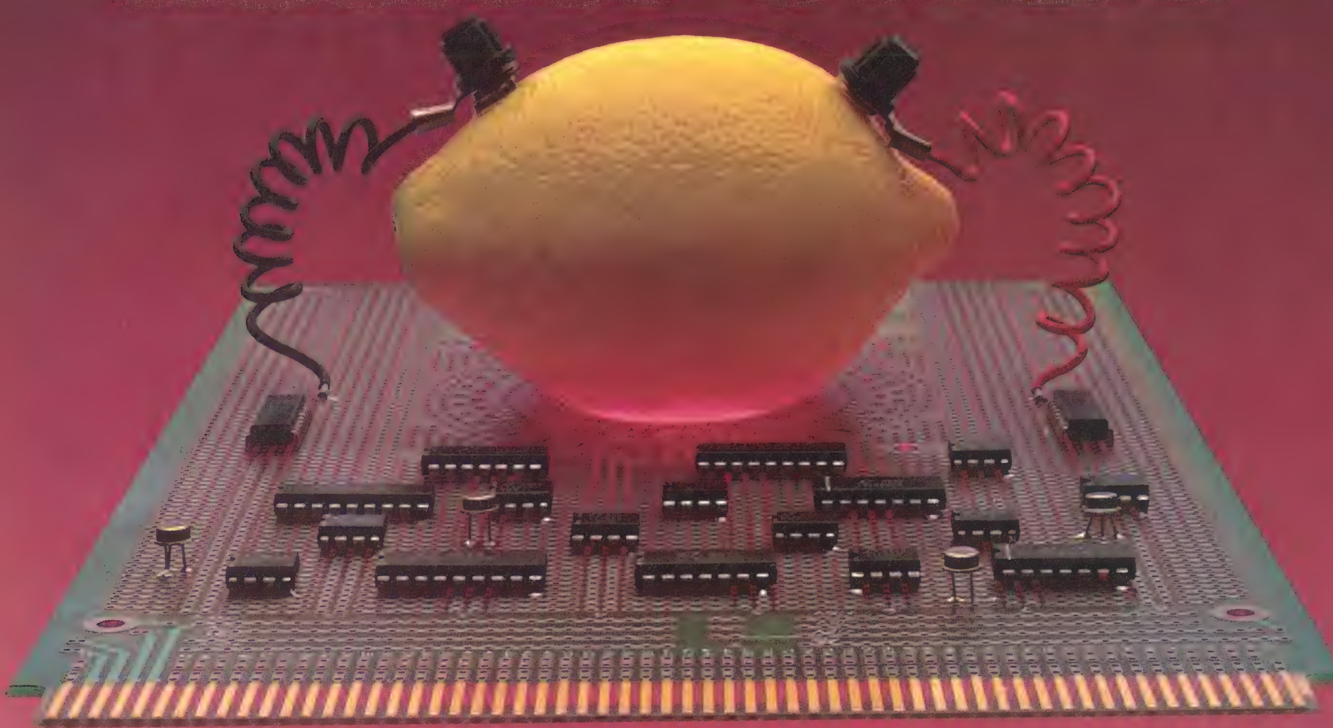

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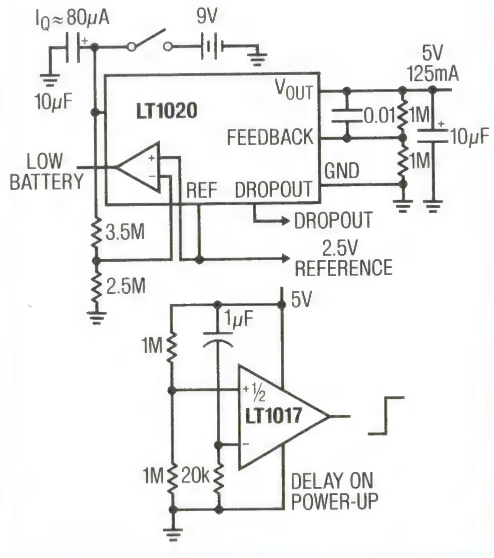

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Versatile ramp generator uses 1k-bit RAM

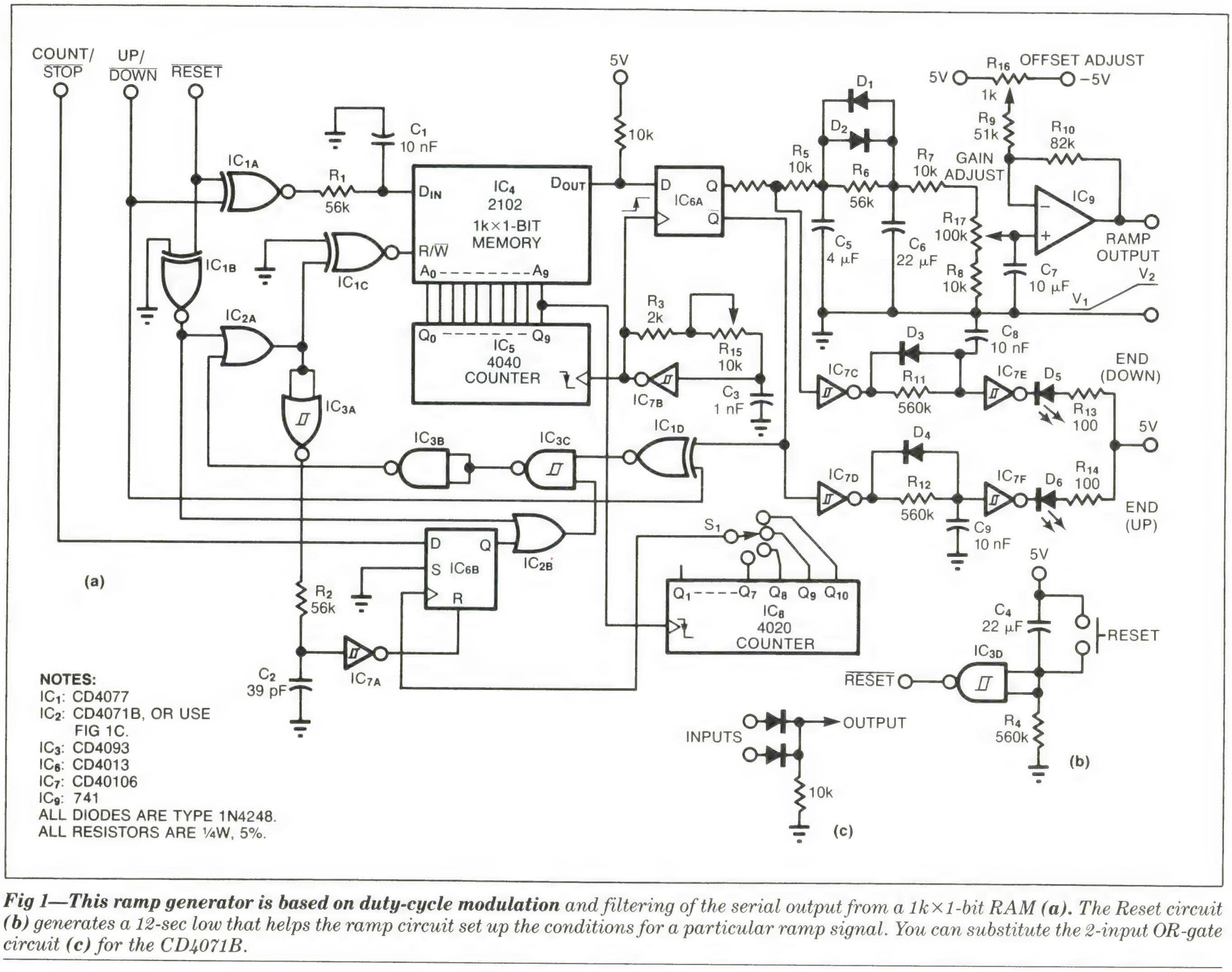
J Martinez and F Sandoval
ETS Ing Telecomunicacion, Madrid, Spain

The ramp generator in **Fig 1** is an alternative to more-expensive approaches that are based on a D/A converter with 12- to 14-bit resolution. The circuit lets you set the ramp's start and stop levels, select up or down (positive or negative slope), adjust the amplitude and repetition rate, and stop at any level on the ramp. IC_4 is a 1k-bit RAM that provides 1024 steps for any ramp regardless of amplitude and duration; for higher resolution, you need a larger memory.

Op amp IC_9 and associated components filter the memory's serial output. By writing ones (or zeros) to the memory at regular intervals, you can steadily increase (or decrease) the average voltage level $n \cdot V_{CC}/1024$ at D_{OUT}, where n is the number of ones in the memory at that moment.

The nominal 200-kHz square wave at IC_{7B}'s output clocks the memory and counter IC_4. The counter generates addresses that scan through each of the memory's 1024 locations about 200 times/sec; the falling edge at counter output Q_9 that occurs on the completion of each scan clocks counter IC_8. The setting of switch S_1 provides coarse selection of the ramp duration (potentiometer R_{15} provides the fine adjustment).

Each positive transition on the wiper of S_1 initiates a memory-write operation by clocking flip-flop IC_{6B}. The write operation changes a zero to one for ascending ramps, or a zero to one for descending ramps. LEDs D_6 and D_5 signal the completion of ascending and descending ramps, respectively.



NOTES:
IC1: CD4077
IC2: CD4071B, OR USE FIG 1C.
IC3: CD4093
IC6: CD4013
IC7: CD40106
IC9: 741
ALL DIODES ARE TYPE 1N4248.
ALL RESISTORS ARE ¼W, 5%.

Fig 1—This ramp generator is based on duty-cycle modulation *and filtering of the serial output from a 1k×1-bit RAM* ***(a)****. The Reset circuit* ***(b)*** *generates a 12-sec low that helps the ramp circuit set up the conditions for a particular ramp signal. You can substitute the 2-input OR-gate circuit* ***(c)*** *for the CD4071B.*

R_2 and C_2 delay the reset of flip-flop IC_{6B} long enough to write into one memory location following each positive transition at the flip-flop's clock input. Also, gates IC_{1D} and IC_{3C} delay the write operation by an increasing amount as the ramp grows, thus allowing time for the readout of those ones (or zeros) written since the ramp began.

When you use the ramp generator in a temperature controller, it can sweep between the temperatures represented by voltages V_1 and V_2, where $V_1<V_2$. First, set Up/$\overline{\text{Down}}$ to 1 (for ascending ramp), and set Count/$\overline{\text{Stop}}$ to 0. Press Reset **(Fig 1b),** which initiates a 12-sec low on $\overline{\text{Reset}}$. The memory fills with zeros, so flip-flop IC_{6A}'s Q output is low and the filter output (the op amp's noninverting input) is 0V. Use the offset-adjust potentiometer (±8V range) to set the op amp's output to V_1. Next, set Up/$\overline{\text{Down}}$ to 0 and press Reset again—the memory fills with ones. The filter output (wiper of R_{17}) is V_{CC}. Set the op amp's output to V_2 using the gain-adjust potentiometer. Then, set Up/$\overline{\text{Down}}$ to 1 and press Reset to fill the memory with zeros again; the generator is ready to run when you set Count/$\overline{\text{Stop}}$ to 1.

Ramp-linearity error is very low, and output ripple is less than 0.03%. Power dissipation is less than 250 mW. Because changes in the supply voltage will affect linearity by altering the frequency at IC_{7B}, you should provide good supply regulation or arrange a clock frequency that isn't affected by the power supply. **EDN**

To Vote For This Design, Circle No 746

Filter IC performs signal demultiplexing

Smaragda Denton
National Semiconductor Corp, Santa Clara, CA

In **Fig 1,** IC_3 is a fourth-order, lowpass Butterworth filter implemented with switched-capacitor techniques. Because the chip samples its filter input only during low clock states, a suitable clock signal can also make the chip behave as a demultiplexer does.

The decoder, IC_2, repeatedly selects each of the four input signals ($V_{IN}1$ to $V_{IN}4$) in turn by asserting a positive pulse at the appropriate terminal of multiplexer IC_1. The resulting time-multiplexed signal at IC_3's filter input appears on an oscilloscope, as shown in the upper trace of **Fig 2b.** By setting switch S_1 to the same decoded waveform that selects input V_3, you obtain a clock signal that enables the filter to respond only to V_3.

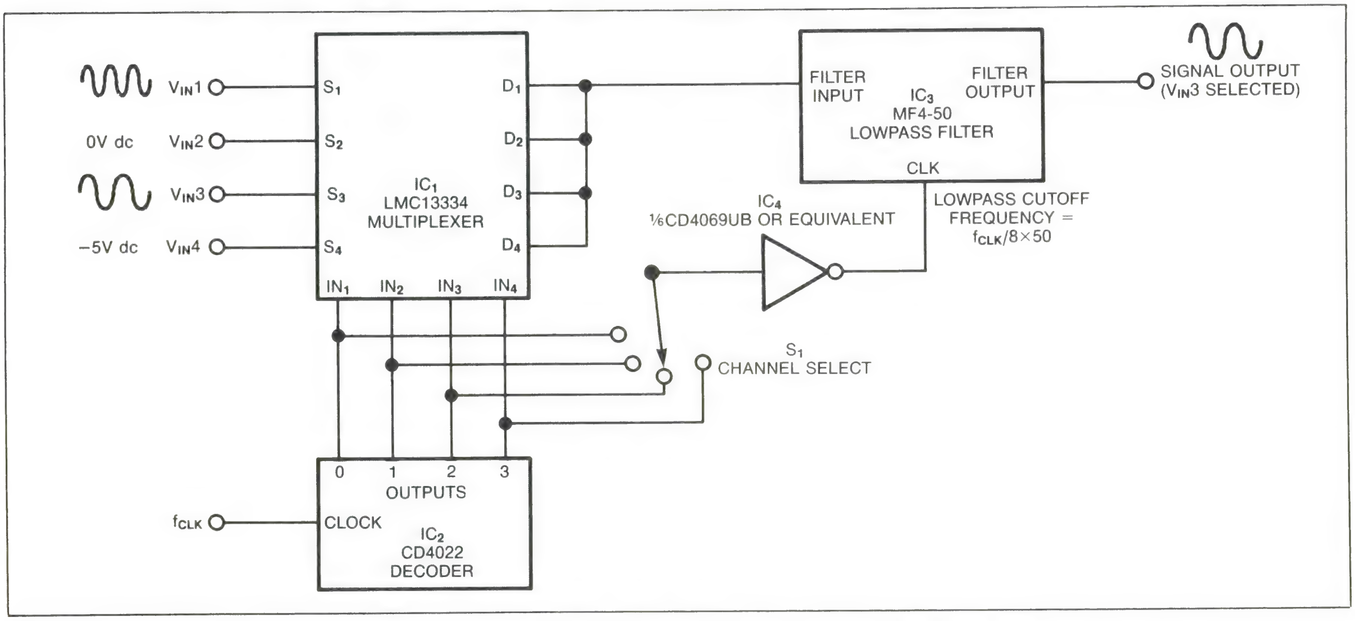


*Fig 1—**The filter chip, IC_3, serves as a demultiplexer** in addition to providing its usual filtering function.*

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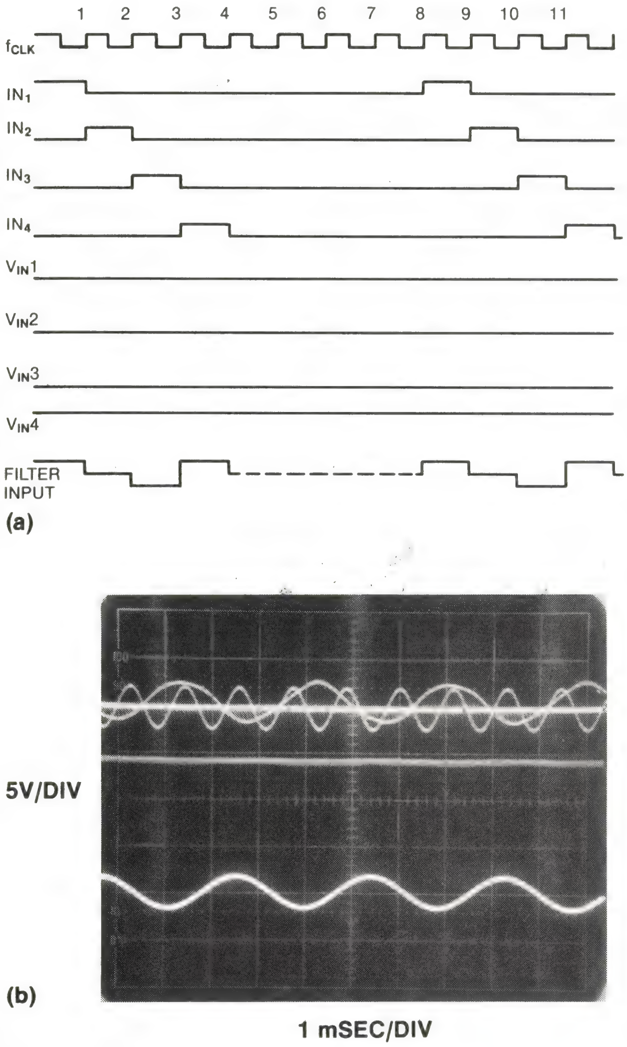

*Fig 2—**This timing diagram (a) shows channel-select signals** and analog input voltages, which appear as dc levels over this short time interval. The trace photo **(b)** shows a multiplexed waveform at the filter input (top trace) and a single-signal output (lower trace).*

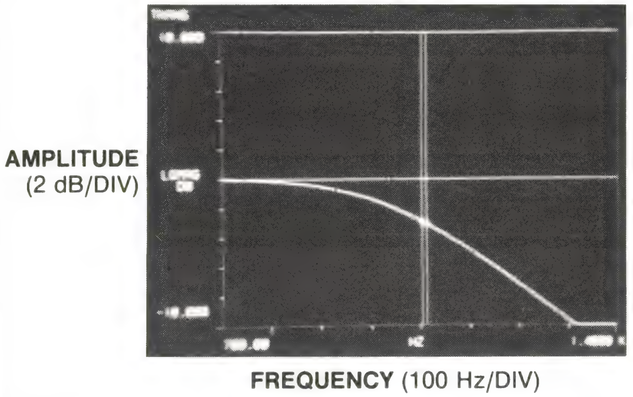

*Fig 3—**A slight amplitude difference is apparent** in filter outputs that use a clock with a 50% duty cycle (upper trace) vs a 12% duty cycle.*

(The filter's switched-capacitor input provides a sample/hold function; the filter doesn't look at its input when the clock is high.) IC_3 then reconstructs and filters the V_3 signal at its filter output.

The filter derives two internal, nonoverlapping clocks from the signal applied at its clock input, thus causing a delay between the external clock's falling edge and the actual analog sampling time. This delay serves as a deglitch interval, allowing the filter to ignore the multiplexer's glitch during channel changes. On the other hand, because the filter's clock signal doesn't have a 50% duty cycle, the filter's cutoff frequency, passband gain, and dc offset do not quite meet MF4 specifications. Using a 100-kHz clock with a 50% duty cycle vs a 12% duty cycle shows a slight reduction in output amplitude corresponding to the lower duty cycle (**Fig 3**). **EDN**

To Vote For This Design, Circle No 748

Ground-noise probe is battery powered

John Darjany
Griffin Technology Inc, Rancho Dominguez, CA

Oscilloscope measurements of ground noise may be unreliable because noise can enter your circuit via the scope's 3-pronged power plug. You can avoid this problem by using the ground-noise tester shown in **Fig 1.** Powered by two 9V batteries, the circuit dissipates power only while its push-to-test switch (S_1) is depressed.

Noise pulses that reach IC_{2A}'s switching threshold (about 1.5 to 1.8V) create a logic transition that triggers the monostable multivibrator IC_3, which stretches the pulse enough to produce a visible blink from LED D_1. You set the noise reference level by adjusting the threshold-adjust potentiometer R_1, which lets the cir-

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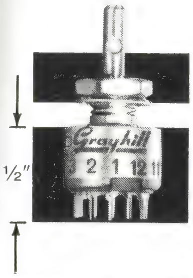

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CIRCLE NO 134

cuit respond to minimum pulse amplitudes ranging from about 0 to 1V. For convenience, you can use a 1-turn potentiometer for R₁ and calibrate the dial by applying an adjustable dc voltage, monitored by an accurate voltmeter. **Fig 2** shows two digital-system applications of the tester. **EDN**

To Vote For This Design, Circle No 750

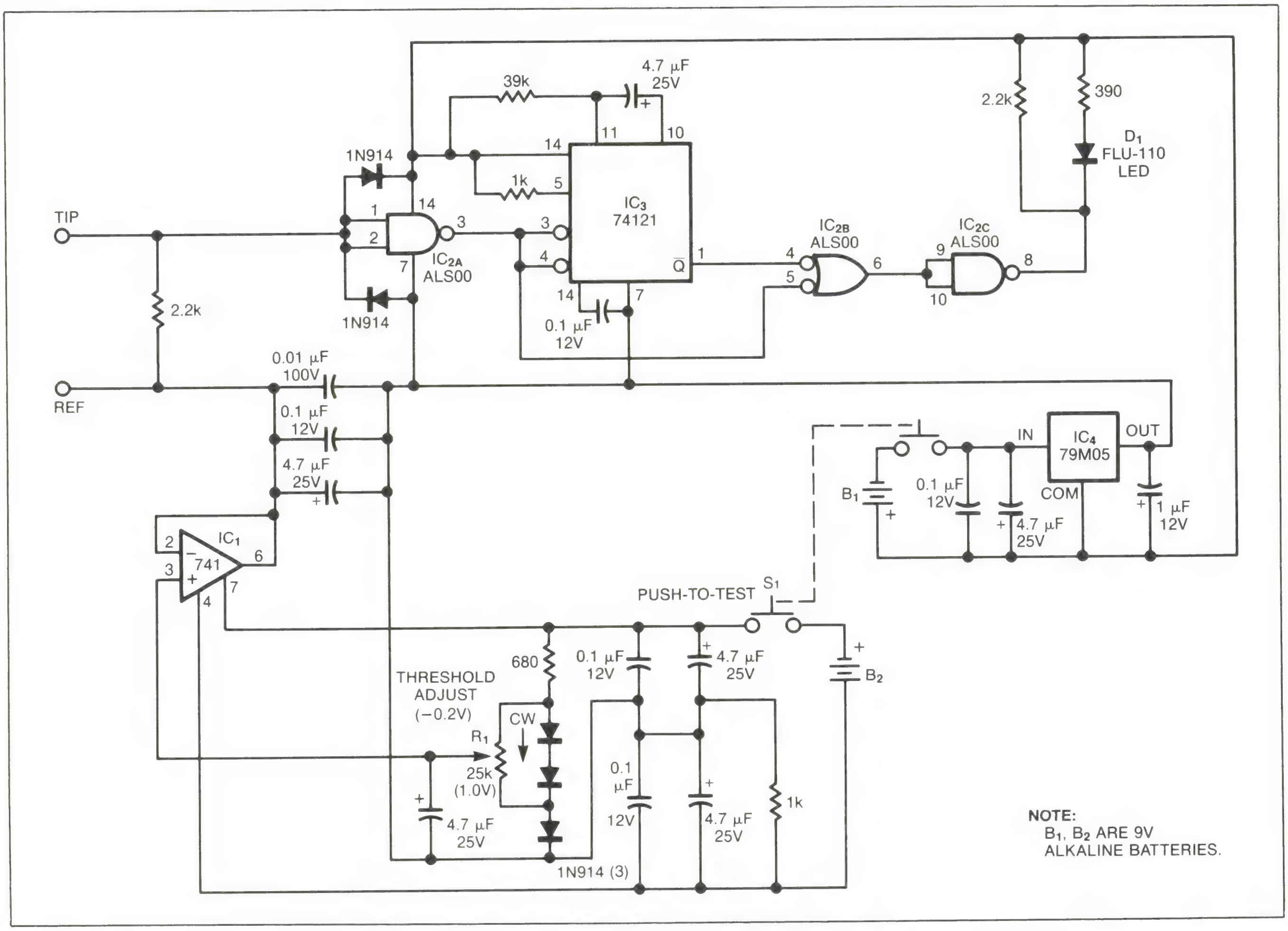


***Fig 1—This ground-noise tester senses voltage excursions** with a minimum threshold ranging from about 0 to 1V.*

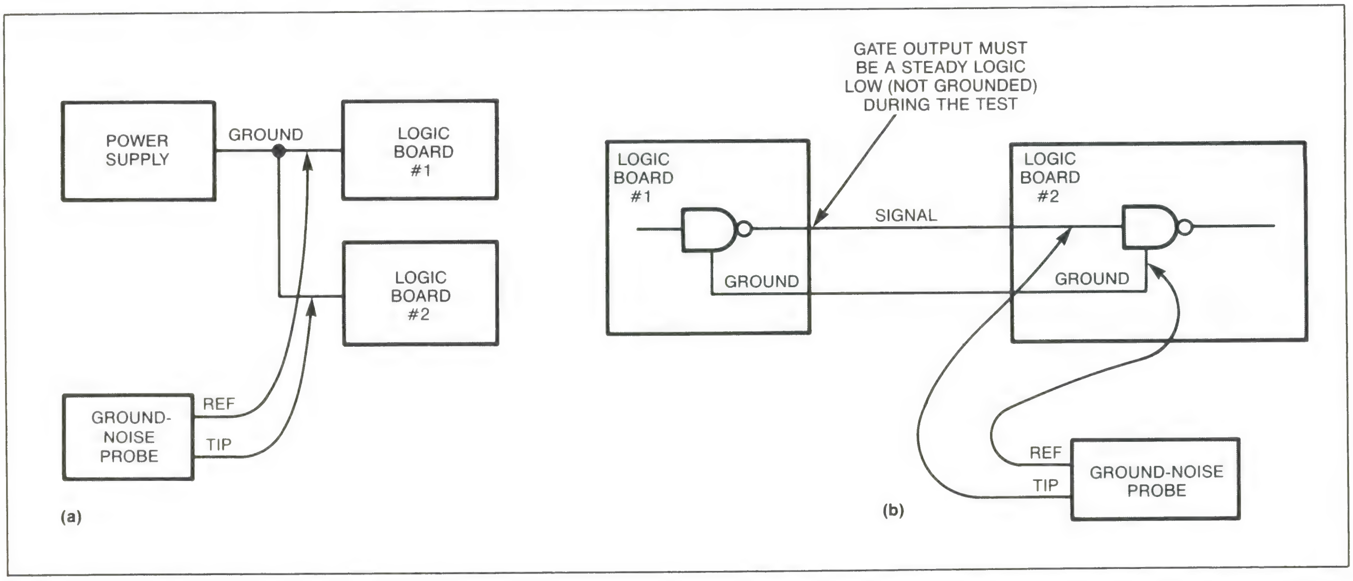
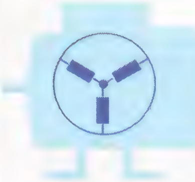


***Fig 2—A ground-noise probe (Fig 1)** makes reliable measurements between ground conductors **(a)** or between logic low and ground **(b)**.*

SIEMENS

Pulse-width modulator SLE 4520:

The three-phase maker



Siemens has come up with an integrated circuit that, combined with an 8-bit microcontroller, makes three-phase current of variable frequency and amplitude out of a rigid single-phase power supply.

Designing a high-performance, low-noise frequency converter thus becomes a lot simpler.

Siemens SLE 4520 helps produce three-phase drives with a variable and wide speed range – straightforward, exactly right for the application and low-cost. **And you don't even need a three – phase supply to do it.**

System highlights:

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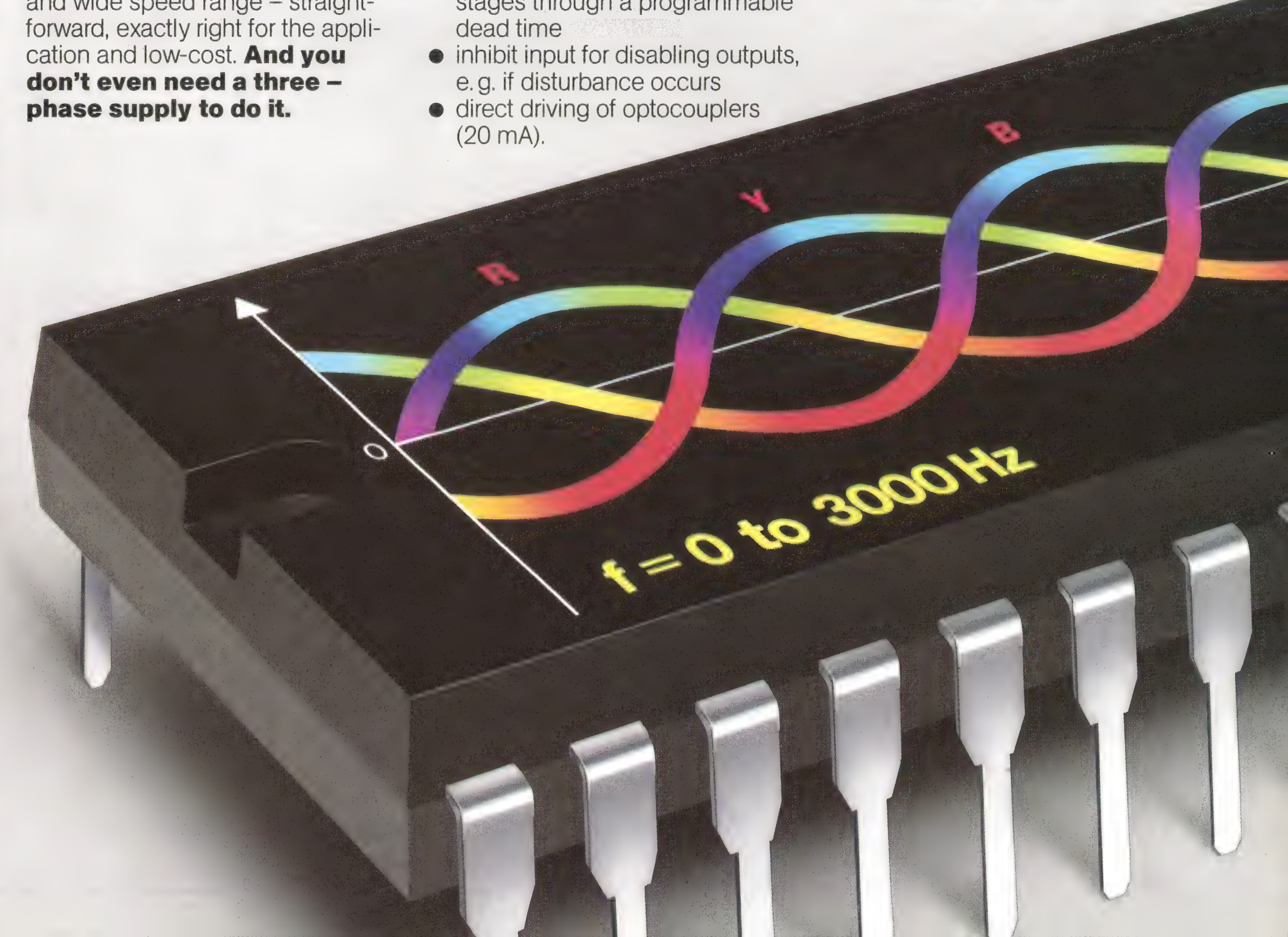
- basic software package for fast development
- motor frequencies from 0 to 3000 Hz and above, with a switching frequency selectable up to 23.4 kHz
- adaptation to different output stages through a programmable dead time
- inhibit input for disabling outputs, e. g. if disturbance occurs
- direct driving of optocouplers (20 mA).

This pulse-width modulator from Siemens is suitable for numerous fields of application, e. g. for constructing conveyor installations, textile machines, pumps, machine tools, printing presses, robots, washing machines, ventilators and to replace universal motors.

If you want to find out more about SLE 4520, write Siemens AG, Infoservice 12/Z016, Postfach 23 48, D-8510 Fürth, West Germany quoting "Pulse-width modulator".

CIRCLE NO 136

12/Z016e



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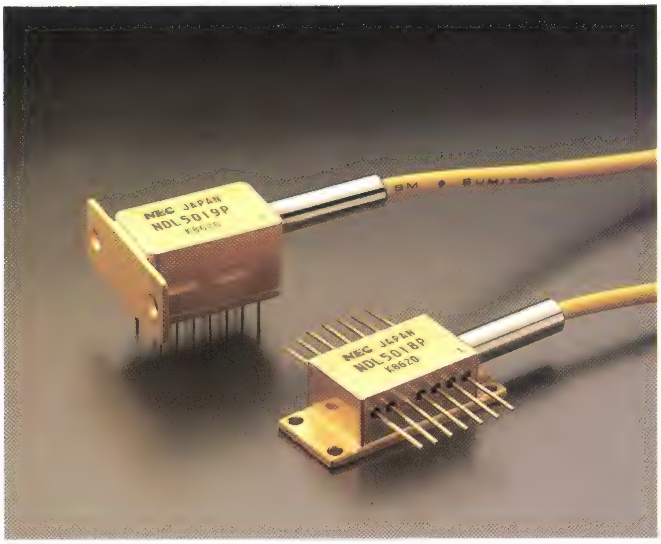
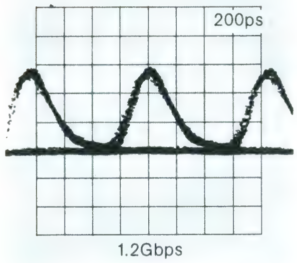
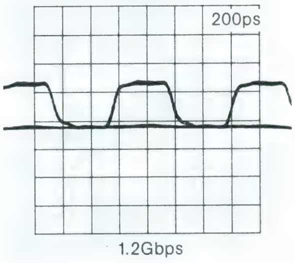


NEC has extended its range of highly successful laser diode modules. The new high-speed, high-reliability laser diodes typically feature 0.2 ns and 0.3 ns rise and fall times, low threshold current and an output power of 1.5 mW in singlemode fiber operation as well as an internal thermoelectric cooler. These features make the NDL5018P and NDL5019P ideal devices for long distance high-capacity transmission systems. The double channel planar buried heterostructure provides the modules with stable fundamental transverse mode operation over a wide temperature range.

The compact laser modules are supplied either in 14-pin dual-in-line or butterfly packages. Both versions match NEC's existing laser modules for a no-problem fit with current system designs.



Optical Response Waveform



Drive Current Waveform

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NEC

CIRCLE NO 138

Sync separator flags odd fields

Luen-Yuan Lin
DRS, Precision Echo Inc, Santa Clara, CA

In 1982, EDN published three Design Ideas that showed how to separate the horizontal and vertical sync pulses from a video composite-sync waveform (**Refs 1, 2, and 3**). The circuit in **Fig 1** also separates the sync pulses, and identifies odd vs even frames as well, by producing a field index pulse (E) for each odd field. Component values are suited for operation on an RS-170 standard waveform (A), but the circuit will operate with other interlaced-scan waveforms if you modify the time constants (t_1 and t_2) associated with one-shots IC_{1A} and IC_{1B}.

The RS-170 standard defines one video frame as two fields of 262.5 lines each. A slight difference in the fields' vertical-interval timing allows them to be distinguished electronically.

Falling edges of the composite-sync input (A) trigger the IC_{1A} one-shot, producing output (B) at the horizontal sync frequency. The one-shot sets the low intervals t_1 in this waveform to $0.5H<t_1<H$, where H is the 63.5-μsec time interval between horizontal lines. Similarly, one-shot IC_{1B} triggers on the rising edges of waveform ($\overline{B}$) to produce a waveform (C) in which the low intervals (t_2) are less than 0.5H.

Flip-flops IC_{2A} and IC_{2B} sample the input (A) on the rising edges of their clock inputs (waveforms (C) and

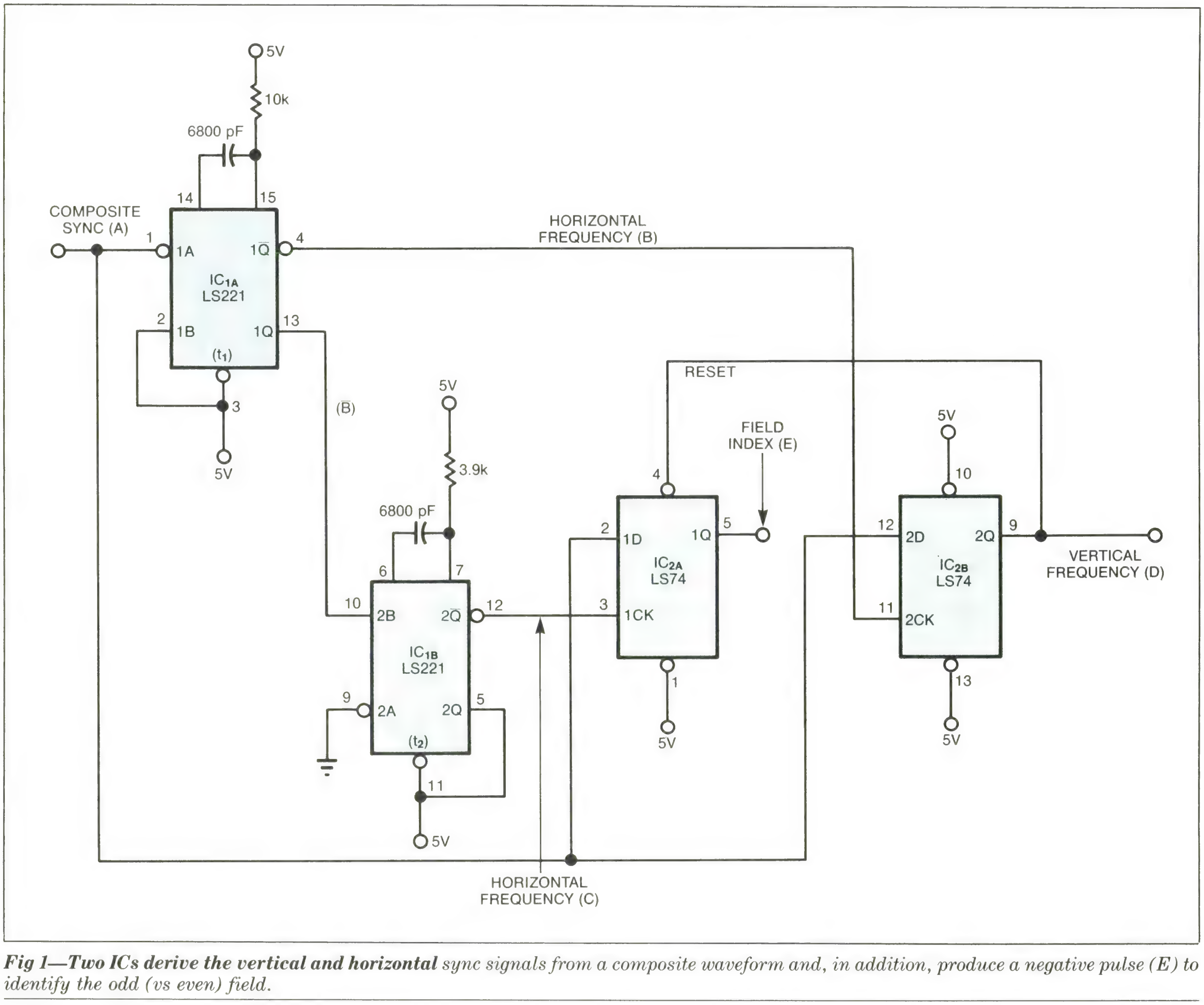

*Fig 1—**Two ICs derive the vertical and horizontal** sync signals from a composite waveform and, in addition, produce a negative pulse (E) to identify the odd (vs even) field.*

(B), respectively). The resulting field index signal (E) remains high during even fields **(Fig 2)**, but produces a negative pulse **(Fig 3)** for odd fields. Use of the vertical frequency (D) as a reset to flip-flop IC_{2A} makes the circuit work; the dashed lines indicate the pulses you will get if this connection is omitted. **EDN**

To Vote For This Design, Circle No 749

References

1. Albing, Bradley, "Sync separator provides speed, accuracy," *EDN*, January 6, 1982, pg 207.
2. Bepko, Stephen J, "Modified sync separator uses fewer ICs," *EDN*, May 26, 1982, pg 204.
3. Gershfeld, Jack, "Sync separator uses only one IC," *EDN*, September 29, 1982, pg 153.

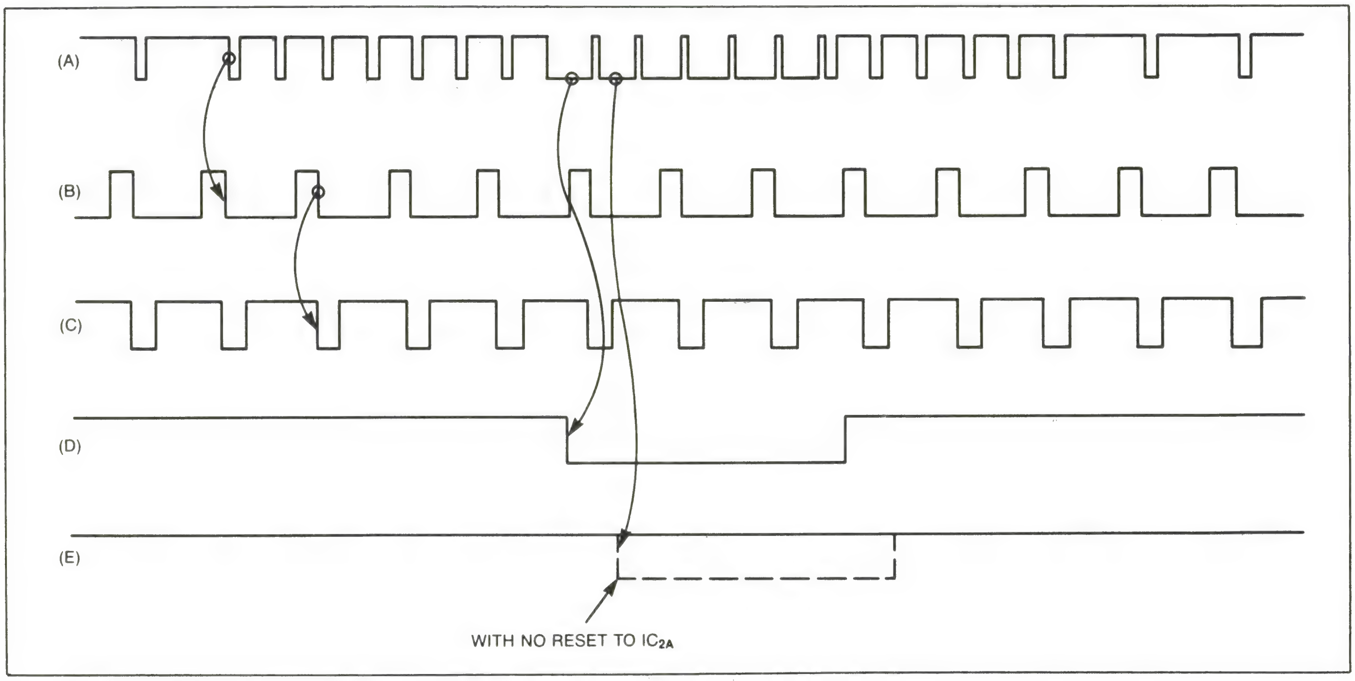

Fig 2—Waveforms show no change in Fig 1's output (E) *at the start of an even field. The dashed lines indicate the pulse that would occur without a reset signal to IC_{2A}.*

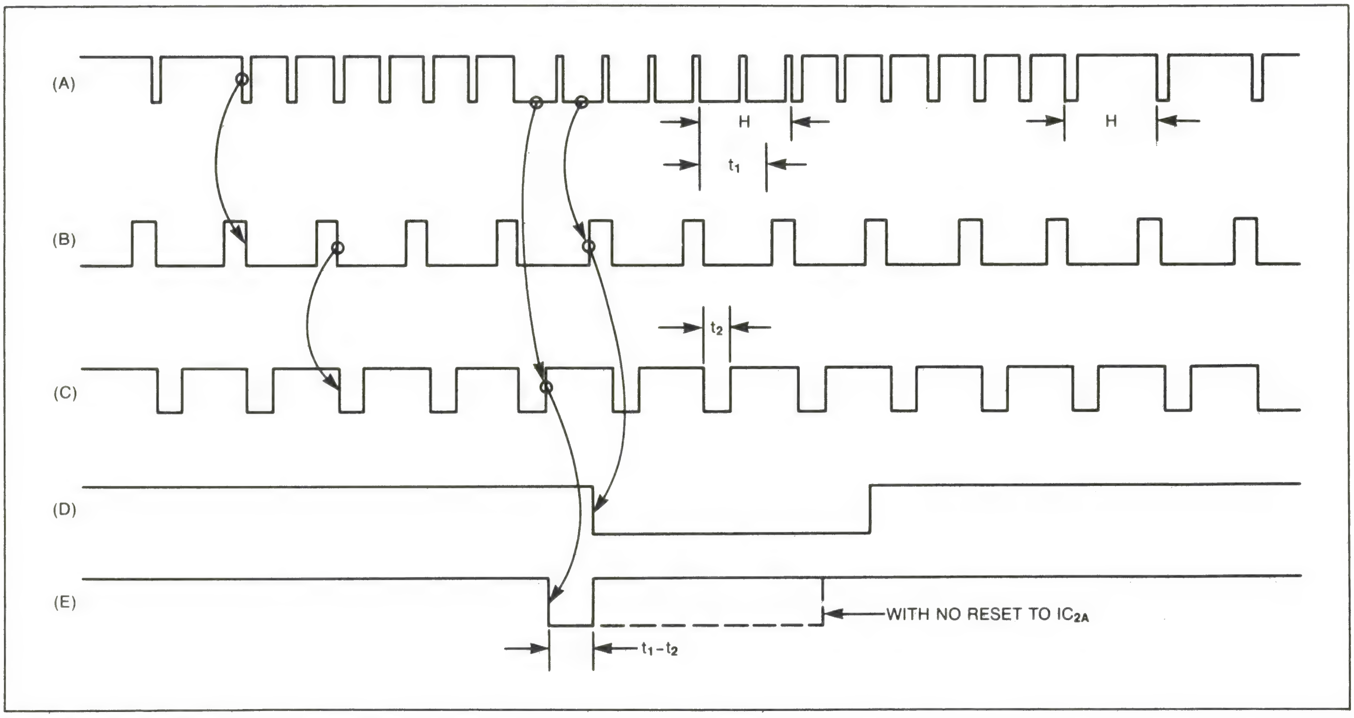

Fig 3—The field index output (E) in Fig 1 *emits a negative pulse only at the beginning of an odd field.*

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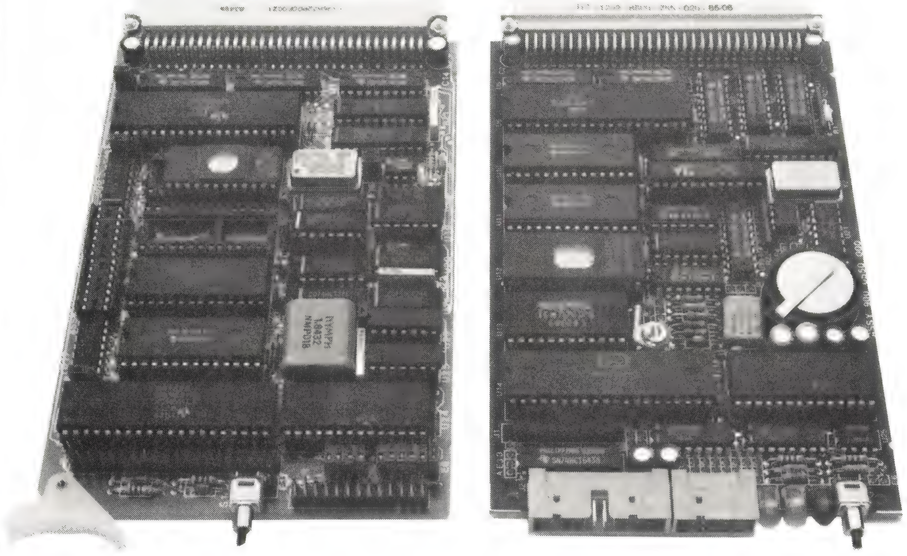

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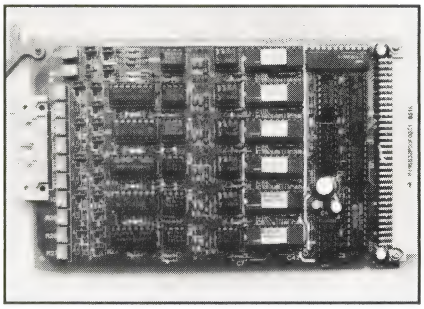
CIRCLE NO 93

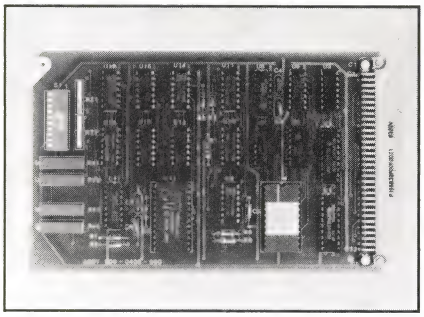
Analog Output Module Supports Multi-Point Control



A digital-to-analog converter module, model RM65-5306E, has six independent channels with 12-bit resolution, to allow multi-point analog control and feedback systems to be implemented with fewer boards, thus lower cost, in a modular microcomputer system. Each of the six channels is selectable for several unipolar or bipolar output ranges. Two pots on each channel provide calibration adjustment. Accepts external reference voltages. Single Eurocard size, RM 65 bus compatible. $450 list price. **Dynatem Inc.**, Irvine, CA.

CIRCLE NO 94

High Throughput Math Co-Processor Module



A math co-processor Module, RM65-2122E, performs fixed point 16- and 32-bit operations or 32-bit floating point operations. Multiply, divide, trigonometric, square root and exponentation functions. One or two Am9511A devices at either 2 or 3 MHz. Completion of operation generates interrupt or status may be polled. User assignable to single page of address space. RM 65 bus compatible, single Eurocard size. $390 list price, delivery from stock. **Dynatem Inc.**, Irvine, CA.

CIRCLE NO 95

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Reset circuit solves brownout problems

Damian G Bonicatto
Hibbing Electronics Co, Hibbing, MN

Most microprocessor systems include some form of power-on reset circuit, such as the simple RC network shown to the right of the dashed line in **Fig 1.** The circuit is satisfactory provided that V_{CC} drops low enough for the capacitor to discharge below the $\overline{\text{Reset}}$ line's minimum input-low level (0.8V, for example). The Reset will never trigger, though, if V_{CC} drops only to, say, 2V and then returns to its normal level. Yet the µP may act irratically while V_{CC} is low.

You can cure this brownout problem by adding Q_1 and R_2 (shown to the left of the dashed line in **Fig 1**). Q_1 is a programmable unijunction transistor (PUJT) whose operation is similar to that of an SCR. With these additions, C_1 supports the anode voltage as V_{CC} drops, and the PUJT will trigger when its gate drops about 0.7V below the anode (unless the V_{CC} change is very gradual). C_1 discharges when the PUJT triggers, which ensures a reset by pulling the Reset line low. **EDN**

To Vote For This Design, Circle No 747

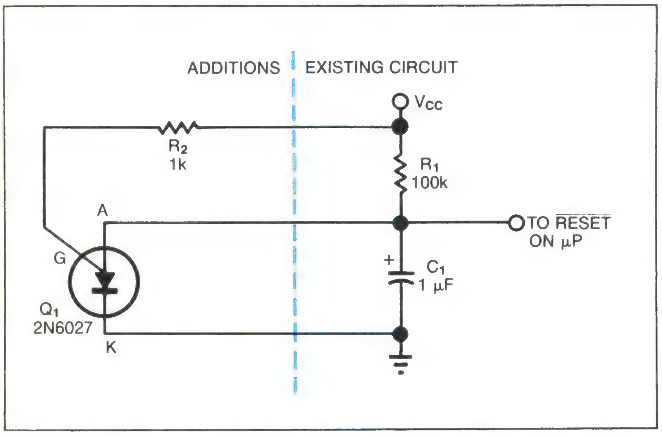

*Fig 1—**This brownout circuit ensures a reset** for V_{CC} excursions that are only 0.7V below nominal.*

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IMS2801-10	Page Mode	53ns	16ns	56ns

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CIRCLE NO 140

Design Ideas Winners January through December 1985

January 10, 1985
Giovanni Stocchino, FATME, Rome, Italy
"Improve voltage-controlled current source."
January 24, 1985
Arthur Delagrange and **Reynold Douyon,** Naval Surface Weapons Center, Dahlgran, VA
"Pocket calculator eases filter design."

February 7, 1985
Fran Hoffart, National Semiconductor Corp, Santa Clara, CA
"Charger extends lead-acid-battery life."
February 21, 1985
Paul Galluzzi, Dynamics Research Corp, Wilmington, MA
"Dual optoisolator detects zero crossings."

March 7, 1985
Tom Lange, Rochester, NY
"Use 3-state buffer as PLL phase detector."
March 21, 1985
Jade Alberkrack, Motorola Semiconductor Products, Phoenix, AZ
"Build step-up/step-down regulator."

April 4, 1985
Johannes Bjorner, Digital Equipment Corp, Marlboro, MA
"Op amp provides accurate level shifter."
April 18, 1985
Mick Murray, Lab-Line Instruments, Franklin Park, IL
"Program calculates best-fit 1% resistors."

May 2, 1985
Al Pshaenich and **Ron Backhaus,** Motorola Power Products Div, Phoenix, AZ
"Storage-time tester uses two ICs."
May 16, 1985
Richard Andelfinger, Hughes Aircraft Co, Tucson, AZ
"Circuit clamps video signals."
May 30, 1985
Christopher Paul, Coherent Communications Systems Group, Dix Hills, NY
"High-gain amp yields low dc output offset."

June 13, 1985
Fred Brown, Consulting Engineer, Lake San Marcos, CA
"Circuit measures capacitor's resistance."
June 27, 1985
Stephen Crum, Service Machine Co, Huntington, WV
"Capacitor maintains data during power loss."

July 11, 1985
Robert D Grappel, Compdata Services Corp, Needham, MA
"C program finds words that sound alike."
July 25, 1985
Andrew Dart, Trans-Texas Telegraph Co, Duncanville, TX
"Program speeds best-fit 1%-resistor calculations."

Winner of the year designs op amp with high-voltage output swing

Barry Kline has won the 1985 Design Ideas grand prize of $1500 for "Enhanced op amp delivers 100V p-p," which appeared in the September 5, 1985, issue of EDN. Using current feedback and four discrete transistors, his circuit increases the output swing of an OP-27 op amp to 100V p-p and higher. Mr Kline won the grand prize, despite some typographical errors that appeared in his equations (see EDN, November 14, 1985, pg 42.)

Though primarily an analog-design engineer with expertise in high-frequency pulse circuits, Mr Kline took on the task of redesigning an unstable servo amplifier in a medical imaging system. His winning Design Idea is the result: An amplifier that drives a 90V dc motor—via a power emitter-follower—which positions a radiation detector housed in a 1500-lb lead "bucket" to block background radiation.

Mr Kline holds a BSEE from Case Western Reserve University in Cleveland, OH. Employed by Transat Corp (Solon, OH) since May, he previously worked for Technicare Corp (also in Solon) for five years as a design engineer. He practices carpentry in his spare time, enjoying everything from house remodeling to cabinet making.

Congratulations, Mr Kline, from all of us at EDN. *—Tarlton Fleming*

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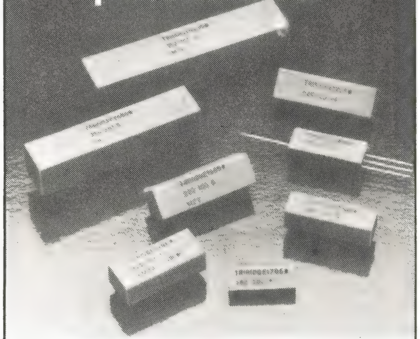

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CIRCLE NO 98

DESIGN IDEAS

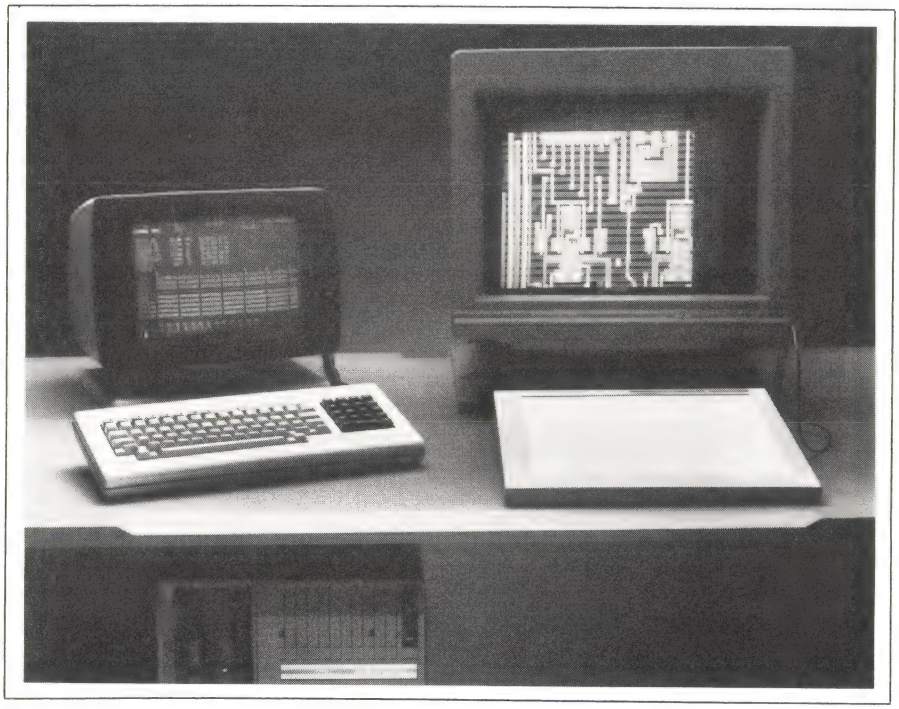
August 8, 1985
Roy Griffin, M/A-Com, El Paso, TX
"Circuit monitors RS-232C communications."
August 22, 1985
S L Black and **H L Maddox,** AT&T Technologies, Columbus, OH
"Simple circuit suits quadrature detection."

September 5, 1985
Barry Kline, Technicare Corp, Solon, OH
"Enhanced op amp delivers 100V p-p."
September 19, 1985
Leo M Almazan, Naval Ocean Systems Center, San Diego, CA
"Perform a Z80 reset without memory loss."

October 3, 1985
Frank Michele, Brno, Czechoslovakia
"Circuit increases frequency to ×1000."
October 17, 1985
Marc Saberi, Masscomp, Westford, MA
"Monitor thermocouples electronically."
October 31, 1985
Shalom Bukimer, Tadiran, Syosset, NY
"Current-folding circuit breaker resets itself."

November 14, 1985
Eric Filseth, National Semiconductor Corp, Santa Clara, CA
"Components enhance amplifier's bandwidth."
November 28, 1985
Robert G Culter, Tektronix Inc, Beaverton, OR
"80m radio transmitter uses power MOSFETs."

December 12, 1985
K S Perianayagam and **U K Kalyanaramudu,** Bharat Electronics Ltd, Jalahalli, Bangalore, India
"'UART forms RS-232C/Centronics interface."



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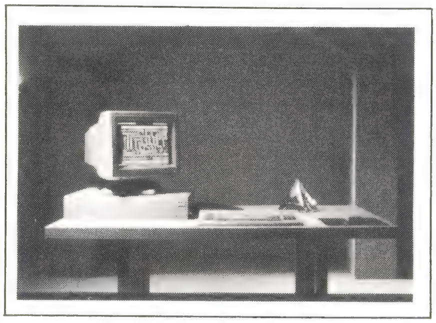
Calma Co, 501 Sycamore Dr, Milpitas, CA 95035. Phone (408) 434-4000.

Circle No 351



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Circle No 352

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- *Cell generators and compilers for semicustom design*
- *Generates logic simulation and timing models*

Vigen provides functional cell generators and compilers for semicustom-IC design. You can compile each configurable cell, with the addition of parameters, into a fully characterized functional structure. The cell generator creates such functions as counters, multiplexers, shift registers, memory (EEPROM, RAM, and ROM), microprocessors, and controllers. The package lets you define such elements as the number of bits in a counter. Using your specifications, the package then produces a schematic-capture symbol, logic-simulation model, and timing model. You can use the compiled cells just as you use any other cell in the company's standard cell library. The configurable cells currently available are counters, PLAs, multiplexers, EEPROMs, shift registers, ROMs, 68C05s, and RAMs. The software runs on Mentor Graphics' Apollo-based workstations. $15,000.

NCR Microelectronics, 2001 Danfield Ct, Fort Collins, CO 80525. Phone (303) 226-9500.

Circle No 353

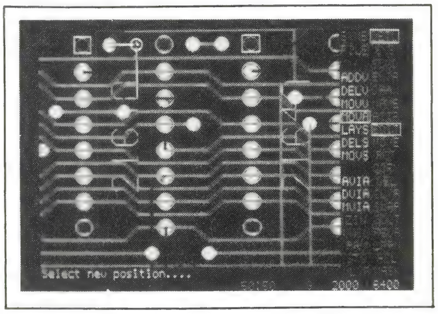
HARDWARE MODELER

- *Plugs into all PMX chassis*
- *Simulations to 25 MHz*

The PMX Fastboard, which plugs into all of the company's PMX chassis, lets you simulate systems at speeds to 25 MHz. It lets you incorporate actual μPs and other VLSI components into a schematic when simulating board- or system-level designs. The board lets you play back stimulus vectors at frequencies of 200 kHz to 25 MHz. You can change vectors in increments of 20 nsec. The 94 logic-signal channels have 64,000-vector depths. $15,000.

Daisy Systems Corp, 700 Middlefield Rd, Mountain View, CA 94039. Phone (415) 960-0123.

Circle No 354



Select new position....

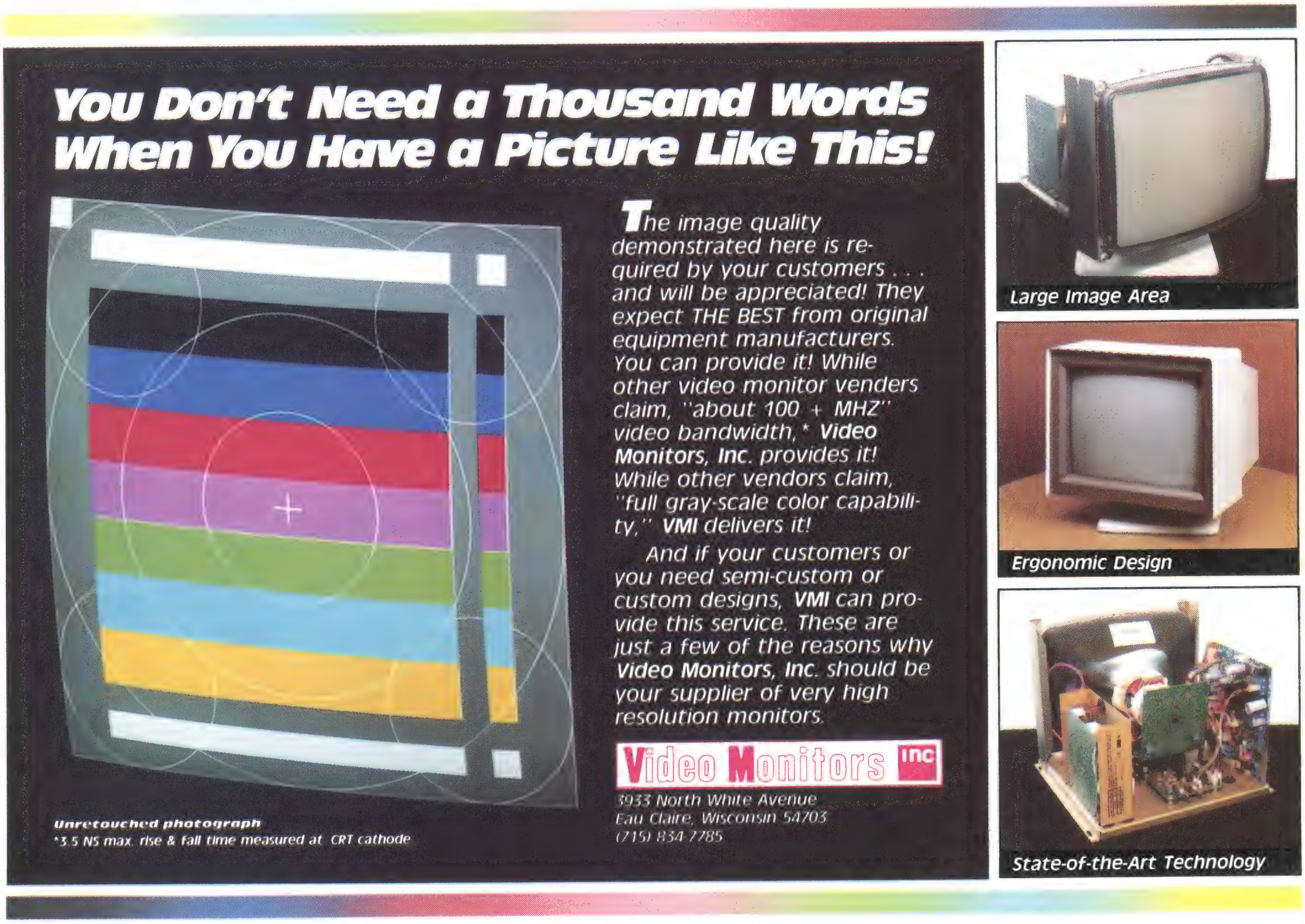
PC-BOARD ROUTER

- *Features 45° routing*
- *Satisfies military requirements such as MIL-STD-275-D*

PC-Route now provides automatic 45° routing. This feature enables you to lay traces in dense areas, such as memory. The feature satisfies military requirements, such as MIL-STD-275-D, that allow notched corners on traces and requires the minimization of trace length. Other features of this autorouter include the ability to set routing priorities by selecting net-list names or components to define the routing area. Two packages include PC-Route Standalone and PCB-3 software. PC-Route Standalone (for new users), $6000; PCB-3, $15,950; update, $480.

Personal CAD Systems Inc, 1290 Parkmoor Ave, San Jose, CA 95126. Phone (408) 971-1300. TLX 3717199.

Circle No 355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Large Image Area
Ergonomic Design
State-of-the-Art Technology

The image quality demonstrated here is required by your customers . . . and will be appreciated! They expect THE BEST from original equipment manufacturers. You can provide it! While other video monitor venders claim, "about 100 + MHZ" video bandwidth,* **Video Monitors, Inc.** provides it! While other vendors claim, "full gray-scale color capability," **VMI** delivers it!

And if your customers or you need semi-custom or custom designs, **VMI** can provide this service. These are just a few of the reasons why **Video Monitors, Inc.** should be your supplier of very high resolution monitors.

Video Monitors INC

3933 North White Avenue
Eau Claire, Wisconsin 54703
(715) 834-7785

Unretouched photograph

*3.5 NS max. rise & fall time measured at CRT cathode

CIRCLE NO 141

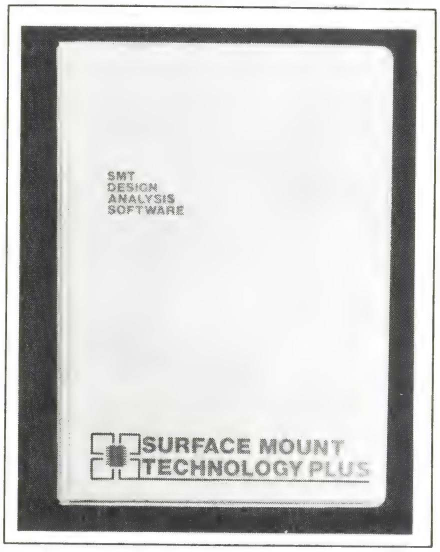
GRAPHICS BOARDS

- *Color and monochrome graphics*
- *Compatible with IBM PC/AT and RT PC graphics adapters*

The Clipper series of raster graphics controllers for the IBM PC/AT and RT PC allows for line-drawing speeds of as much as 10M pixels/sec. This 2-board set is compatible with IBM's Professional Graphics Adapter and Color Graphics Adapter. The boards offer DMA to and from the main memory; color and monochrome displays; pan and zoom; and variable arcs, ellipses, and circles. The required monitor must spec a 19-in. diagonal, a 1280×1024-pixel resolution, and a redraw rate of 60 frames/sec (noninterlaced). The IBM PC character set is standard. Third-party software provides for Tektronix 41xx emulation, DEC VT100 emulation, and the Graphics Kernel System (GKS). $4500.

Small System Design Inc, 225A Lowell Rd, Hudson, NH 03051. Phone (603) 880-1322.

Circle No 396



SMD DESIGN

- *Determines board density and size*
- *Decides whether board should be single- or double-sided*

Surface Mount Design Analysis Software determines whether a surface-mount board should be single- or double-sided, predicts the number of pc-board layers, and calculates the density and size of the board. The board-size calculations include any unused area and the area used for holes, cutouts, and hardware. To perform these calculations, the program requires the number of SMD packages and connector pins. Tables in the program contain the areas of every SMD and DIP component. $350.

Surface Mount Technology Plus, 1786 Technology Dr, San Jose, CA 95110. Phone (408) 287-1247.

Circle No 397

PC-BOARD LAYOUT

- *Produces a standard Gerber-format photoplotter file*
- *Turnkey system includes IBM PC/XT compatible*

This system provides schematic captures and layout for pc boards. It includes an IBM PC/XT compatible, a graphics coprocessor with 2M bytes of memory, and a 14-in. color display with a 640×480-pixel resolution. The PC comes with 256k bytes of memory, a 360k-byte floppy-disk drive, a 20M-byte hard-disk drive, and a 3-button mouse. The software automatically creates net lists, parts lists, design-rule checks, schematics, and pc-board artwork. You run the software on the company's coprocessor board, which plugs into a PC. The design-rule check verifies clearances for any portion of the board. The package lets you vary grid spacings and lay out as many as 30 pc-board layers. Symbolic part libraries are included. You can transfer layouts to pen plotters or Gerber photoplotters. The interactive placement editor lets you use a rat's nest display to reduce the length of interconnections. $10,000.

Modula Corp, 1673 W 820 N, Provo, UT 84601. Phone (800) 545-4842; in UT, (801) 375-7400.

Circle No 398

THE BOARD LEVEL PC BUS BY I-BUS.

We Speak Systems.

Get your dedicated system to market *months* sooner with the PC Bus or PC-AT Bus. The full board-level, passive backplane implementation by I-Bus lets you plug together system components from hundreds of PC Bus manufacturers, and directly execute software developed on and for the IBM® PC and PC-AT.

I-Bus has 4 CPU cards with up to 256K of on-board EPROM space for dedicated applications, and with PROMDISK, you don't even need to produce ROMable code. We have the most complete line of system packaging for the PC/PC-AT Bus, too. All you add are your favorite PC expansion cards for your application.

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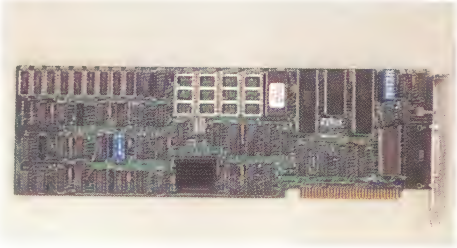

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I-BUS
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(619) 569-0646 Telex: 910 240 0290
CIRCLE NO 101

Our New Emulator's Best Feature...
Its Number of Features

Four events for break and trigger conditions. Each event is set as a bit pattern, including don't care conditions of address, data, status and 16 external lines.

Two 4K×72 bit trace buffers.

16 External trace lines and 2 external trigger out signals.

256K byte emulation memory standard, 1M byte and battery backup optional.

Pass counters can be set for 1-65535 counts for each event.

Opcode execution circuitry filters out unused pre-fetched data.

Interval timer measures the elapsed time from one event to another.

Two RS232 ports.

Trace qualification to allow selective tracing.

Real-time emulation and single-step.

Complex break and trigger points: A then B then C then D, A then B without C.

Symbolic and Source level debuggers to run on IBM PC family or UNIX systems.

Standard battery backup memory for retaining user set-ups.

User interface combines menus and command line control to provide the optimum combination of speed and convenience to quickly isolate system faults.

HMI

The HMI-200 series of microprocessor in-circuit emulators combine all of the features of an emulator and a powerful logic analyzer while utilizing your own IBM PC family or UNIX-based computer. These emulators are a result of HMI's years of experience in the design and application of emulators for all popular microprocessors and offer performance and capability that is unexcelled. Units are initially available to support the 68000 family (68000, 68008 and 68010) and the 64180.

And one more big plus, HMI *delivers* technical support that others only talk about. For complete technical information write to, Huntsville Microsystems, Inc., P.O. Box 12415, 4040 South Memorial Parkway, Huntsville, AL 35802, or call (205) 881-6005. TWX 510-600-8258.

Other HMI Emulators:

8051	8088	6502	6809	8085
8031	8086	Z80	NSC800	8045

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Z80 is a registered trademark of Zilog, Inc.

UNIX is a trademark of AT&T Bell Laboratories, Inc.

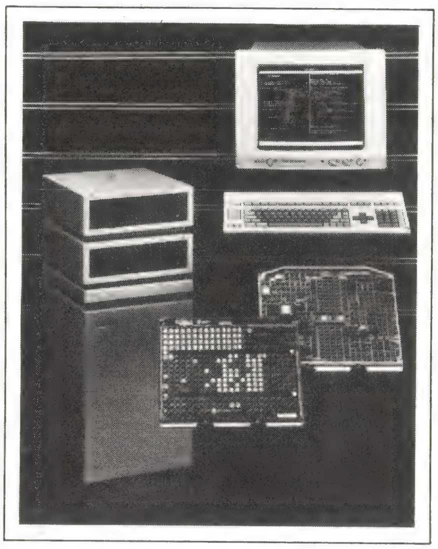
CIRCLE NO 143

COMPUTERS & PERIPHERALS

MULTIPROCESSOR

- *Combines symbolic and numeric processing*
- *Based on 16.67-MHz 68020 CPUs*

Designed to perform both symbolic and numeric processing on the same computer, the Explorer LX links Lisp and 68020 μPs with a set of software tools. The computer's Lisp processor runs Common Lisp; the 68020 μP runs an implementation of Unix System V. Because the μPs share memory, they can both access all the system's data. The system's multiple windowing capabilities facilitate multitasking. A base configuration includes a Lisp processor, 4M bytes of RAM, a 68020 μP with 2M bytes of onboard memory, two 182M-byte hard-disk drives, and an Ethernet interface or cartridge tape. An LX processor upgrade for standard Explorer computers is available. Standard configuration, $73,900. LX upgrade, $18,500.



Texas Instruments Inc, Data Systems Group, Box 809063, H-881, Dallas, TX 75380. Phone (800) 527-3500.

Circle No 356

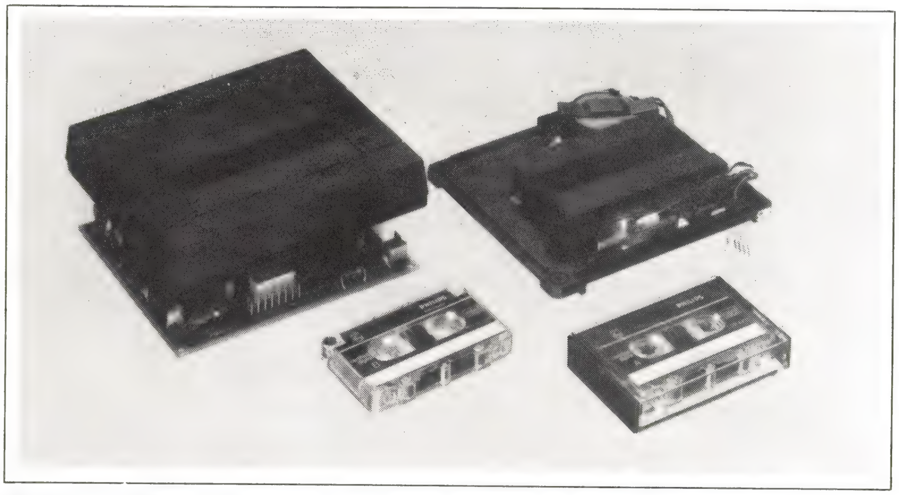
PARALLEL PROCESSOR

- *Can have 5 to 256 processing nodes*
- *Uses two 10-MHz 32016 μPs per node*

The LDF 100 is a parallel-processing real-time computer that incorporates five to 256 processing nodes. It uses a data-driven parallel-processing architecture. The computer automatically distributes data across its available μPs, so you don't have to write the software to distribute the processing across the available nodes. Each processing node has two 16-bit 32016 μPs running at 10 MHz, a 32081 floating-point processor, and 128k to 512k bytes of static RAM. You can order main memory in 2M-byte increments. One μP manages the architecture, and the other runs the application programs. From $67,000.

Loral Instrumentation, 8401 Arrow Drive, San Diego, CA 92123. Phone (619) 560-5880.

Circle No 358



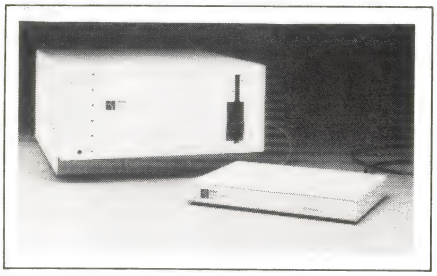
TINY TAPE DRIVE

- *200k bytes of removable data storage*
- *3×3×1.1-in. package*

The MDCR is a miniature data cassette recorder that can store as much as 200k bytes of data on a removable tape cassette. The device measures 3×3×1.1 in. and runs from 12V dc. Its 9600-bps data transfer rate lets you read a fully recorded cassette in 95 sec with less than one hard error per 10^9 bits. The manufacturer reports an MTBF of 5000 hours and a 30-minute MTTR for this unit. This drive comes with an R/W amplifier and motion-control logic. $60 (OEM qty).

Analog & Digital Peripherals Inc, 815 Diana Dr, Troy, OH 45373. Phone (513) 339-2241. TWX 810-450-2685.

Circle No 357



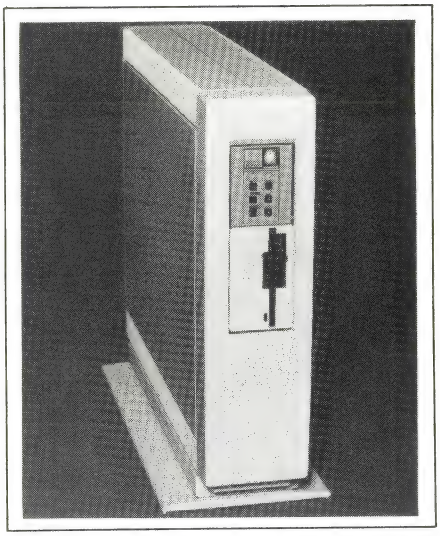
BROADBAND LAN

- *Uses TCP/IP protocols*
- *6-MHz channels*

The CS/1B, MB/1, CR/5, and RFM/5 constitute a family of broadband LAN products that use the high-level TCP/IP communications protocol. Operating at 5M bps on 6-MHz channels, these four devices implement the CSMA/CD access mechanism for high-speed data communications. The CS/1B is a modular communications server that links eight to 32 devices to your broadband LAN. The MB/1 is an 8-port bridge that gives Ethernet-based products access to your broadband network. The CR/5 is a channel remodulator that performs packet regeneration, frequency translation, and collision detection. The RFM/5 modem is an intelligent RF interface. MB/1, $10,500; 32-port CS/1B, $15,600; CR/5, $5000; RFM/5, $795.

Bridge Communications Inc, 2081 Stierlin Rd, Mountain View, CA 94043. Phone (415) 969-4400. TLX 176544.

Circle No 359



REAL-TIME COMPUTER

- *Can handle as many as eight users simultaneously*
- *Contains a 15-MHz version of the J-11 μP*

The MicroPDP-11/53 features a 15-MHz version of the manufacturer's proprietary J-11 μP. The computer can handle as many as eight users simultaneously. Its software is compatible with other PDP-11 computers. However, this model is the first in its family to have a single-board μP with 0.5M bytes of memory on the processor board. You can expand the system to 4M bytes of memory. The unit's three half-height disk drives provide as much as 41.2M bytes of data storage—in your choice of 1.2M-byte floppy-disk drives or 20M-byte Winchester drives. A basic system includes a single-board computer with 512k bytes of RAM and two serial-line ports, a 20M-byte Winchester drive, a 1.2M-byte floppy-disk drive, and an 8-slot rack-mount enclosure. From $9270.

Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Phone local office.

Circle No 360

Silicone rubber gaskets and seals for EMI/RFI Shielding.

Molded parts . . .
or extrusions
Free form . . .
or bonded to metal

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SILICONE RUBBER GASKETING PRODUCTS

- Gaskets and seals for control of electrical interference.
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- Available either "free form" or "supported" with the silicone part permanently bonded to a metal strip or component.

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Silicone, perhaps our most efficient material for EMI/RFI shielding seals, is in a class by itself in resistance to ozone, ultra-violet light and other weathering influences. And Vanshield's special carbon formulations provide superior conductivity with volume resistivities as low as 1 ohm • cm. Operating temperatures range from −100°F to +550°F (−73°C to +288°C).

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CIRCLE NO 144

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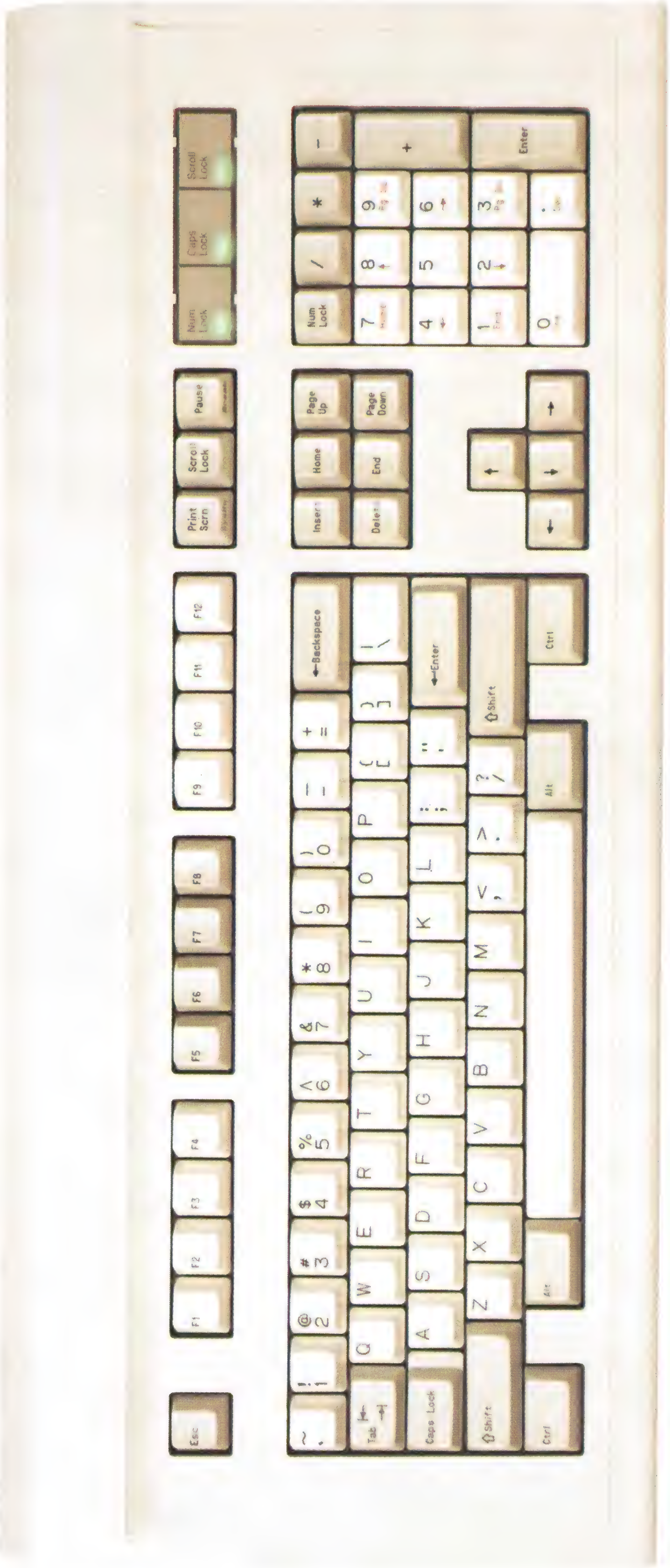

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The Key Tronic
101
KEYBOARD

Act now! Key Tronic has the new IBM* enhanced keyboard layout for you! With responsiveness that's the best in the industry, Key Tronic provides a 101 keyboard which:

- **Features IBM* enhanced layout.**
- **Includes Key Tronic reliable switch technology and quality.**
- **Is ready for shipment now!**

If you want the IBM* enhanced layout, the Key Tronic 101 keyboard is for you. If the 101 is not for you, we have alternative layouts available for immediate shipment. Of course, customized versions are also available.

Contact your Key Tronic Representative today or call OEM Sales at (509) 928-8000 for more information.

The Key Tronic 101 layout features include:

- Separate cursor & numeric pad
- LED indicators
- 12 function keys
- Break over tactile feel
- 19 mm low profile design
- 5 VDC operation

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CIRCLE NO 184

DDC NEWS
ABOUT SYNCHRO-CONVERSION • HIGH-SPEED, HIGH ACCURACY D/A & A/D CONVERSION • DATA BUS DEVICES
PUBLISHED BY ILC DATA DEVICE CORPORATION OCTOBER 1986

MIL-STD-1553 PRODUCTS? ONLY DDC CAN MEET 883 REV C

RECENT CHANGES TO MIL-M-38510, MIL-STD-883, AND MIL-STD-454 AFFECT MILITARY EQUIPMENT MANUFACTURERS

A number of very subtle changes have taken place, which will influence prime government contractors using hybrid microelectronic devices. These subtle changes have been brought about by the need for improved quality and reliability through the issuance of MIL-STD-883C in August 1983 along with MIL-M-38510F in September 1983. In addition, MIL-STD-1772 issued 15 May 1985 and Requirement 64 of MIL-STD-454J issued 30 June 1985 have further supported significant procurement policy changes. **The most subtle and most profound change was the issuance of Notice 4 in November 1985 to MIL-STD-883C which mandates the implementation of MIL-STD-1772 for Hybrid Microcircuit procurement by 29 November 1986.** If you are the recipient of any prime government contract or subcontract after the indicated issuance dates of any of the above cited specifications, then you are obligated to comply with the latest referenced requirements. There are some exceptions, they are, however diminishing, which permit the use of earlier specification revision compliance.

MIL-M-383510F, with expanded Appendix G, provided more realistic requirements for Hybrid Microcircuit. MIL-STD-883C with its now famous "truth in advertising" paragraph (1.2.1) revolutionized the Hybrid Manufacturing industry. **It is no longer permitted to imply compliance with the "intent" of applicable documents; it is necessary to demonstrate "total" compliance with every aspect of the applicable documents.** Requirement 64 of MIL-STD-454 forces procurement of Hybrid Microcircuits to Appendix G of MIL-M-38510 and thereby also forces compliance with MIL-STD-1772. MIL-STD-1772 is a unique standard in that it provides the vehicle for the government to audit Hybrid Microcircuit Manufacturing facilities for compliance to MIL-STD-883 Test Methods (Section A) and requires the Hybrid Microcircuit Manufacturers to qualify their parts, materials, and processes, (Section B) to demonstrate adequacy for military end usage.

When a system or equipment manufacturer purchases Hybrid Microcircuits for military end usage, it must be demonstrated that the Hybrid Manufacturer has, as a minimum:

1. Complete characterization data on the device.
2. Can demonstrate full compliance to Method 5008 of MIL-STD-883 in regard to:
   - —Element Evaluation for Active and Passive elements as well as packages.
   - —Process Control
   - —Screening
   - —Quality Conformance Inspection (Groups A, B, C, and D testing)
3. Is compliant to the general requirements of MIL-STD-883 in regard to:
   - —Environmental Control
   - —Static Control
   - —Test Conditions
   - —Visual Criteria

DESC has now made it easy for system equipment manufacturers to identify those Hybrid Microcircuit Manufacturers that have demonstrated compliance to MIL-STD-1772. The Custom Hybrid Manufacturer's List (QML-38510) was issued on 31 March 1986. Manufacturers shown on this list have been Certified to Section A and Qualified to Section B of MIL-STD-1772.

System and equipment manufacturers not using Hybrid Microcircuit facilities listed on QML-38510 run the risk of having parts procured from non-QML sources disapproved or requiring very costly qualification testing imposed on these non-QML sourced parts.

Contact us for a free copy of the application note "Understanding Quality Conformance Inspection of Hybrid Microcircuits." ☐

DDC
CERTIFIED AND
QUALIFIED TO
MIL-STD-1772

DDC
ILC DATA DEVICE CORPORATION

HEADQUARTERS AND MAIN PLANT: ILC Data Device Corporation, 105 Wilbur Place, Bohemia, N.Y. 11716, (516) 567-5600, TWX: 510-228-7324
WEST COAST (CALIF.): WOODLAND HILLS, (818) 992-1772, TWX: 910-499-2674; SANTA CLARA, (408) 244-0831, TLX: 172775; HUNTINGTON BEACH, (714) 840-5723
WASHINGTON, D.C. AREA: (703) 893-7989, TWX: 910-997-0967; **NORTHERN NEW JERSEY:** (201) 785-1734, TWX: 130-332
EUROPEAN OFFICE: 01-387 4599, TLX: 851-261967; **UNITED KINGDOM:** (44) 635-40158, TLX: 851-848826; **FRANCE:** (1) 4-333-5888, TLX: 842-630609
WEST GERMANY: (08191) 3105, TLX: 841-527128; **SWEDEN:** 46-8-920-635, TLX: 854-10952; **JAPAN:** (03) 490-0203, TLX: 781-34158

Circle No. 5 For Sales Contact

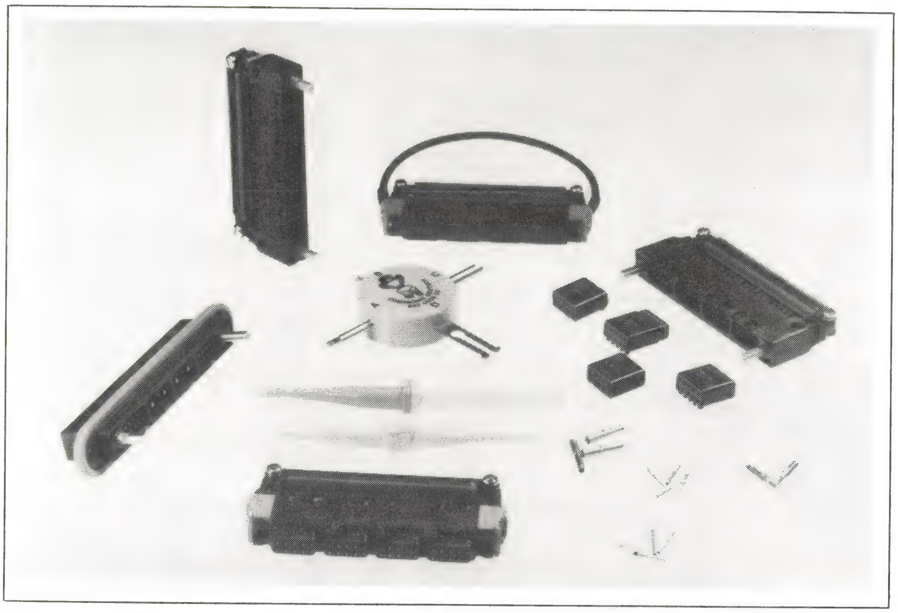
Circle No. 44 For Literature

NEW PRODUCTS

COMPONENTS & PACKAGING

CONNECTORS

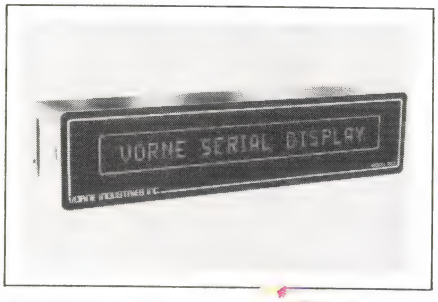
- *Crimp-type MIL-C-39029/22 contacts*
- *400 size-22 contacts fit in 3⅛×2½×4-in. area*



Designed for high-density applications where corrosion resistance, light weight, and small size are critical, DMC connectors are push-pull, rectangular types that use environmentally sealed, crimp-type contacts. The devices' MIL-C-39029/22 contacts release in the rear. Stacking and side-by-side designs allow densities of 400 size-22 contacts in a space measuring 3⅛×2½×4 in. The devices are available in plug-and-cable or box-mounted receptacles that contain four side-by-side, mounted, sealed modules containing the contacts. A redundant polarization system within each module provides 40 keying combinations. Two insertion arrangements are available: Module 40 features 10 size-22 contacts, and module 44 contains two size-16 and two size-22 contacts. Service ratings include a dielectric withstanding voltage of 1500V ac at sea level with an insulation resistance of 5000 MΩ min at 25°C. Maximum current rating for the size-22 contact is 5A; for the size-16 device, 13A. Temperature range is −55 to +175°C. Coupling durability is 250 cycles. The contacts are a gold-plated copper alloy. Depending on configuration and unit quantity, $60 to $150. Delivery, six to eight weeks ARO.

Deutsch Engineered Connecting Devices, Municipal Airport, Banning, CA 92220. Phone (714) 849-7822.

Circle No 361



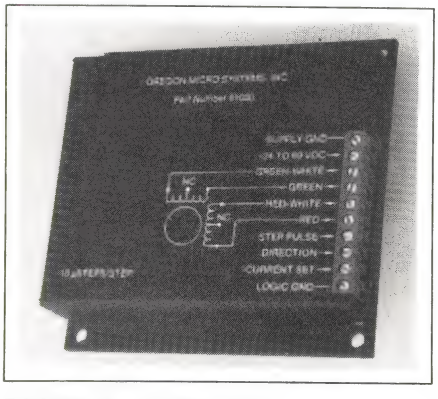
DISPLAYS

- *Provide a single line of 20 characters*
- *Can be part of a network*

You can use these serial-input, alphanumeric, single-line, 20-character displays, the 2000S Series, either as single stand-alone displays or as part of a network in which the displays can be distant from one another. A 2-wire bus connects to the display via TTL, current-loop, RS-232C, RS-422, or RS-485 interfaces, allowing transfer at baud rates of 300, 1200, 2400, 4800, or 9600. By using internal DIP switches, you can individually address as many as 98 displays on the 2-wire bus. Each display has a plug-in communications board that determines the type of serial input the unit accepts and the type of serial output the unit retransmits. A 5×7-dot matrix forms the characters. Character height can be 0.2, 0.35, or 0.59 in.; respective enclosure sizes are 7.2×2.8×4.2, 10×3.1×4.8, and 13.6×3.2×4.8 in. 2005S, $325; 2009S, $355; 2015S, $380.

Vorne Industries Inc, 5831 N Northwest Hwy, Chicago, IL 60631. Phone (312) 775-9440.

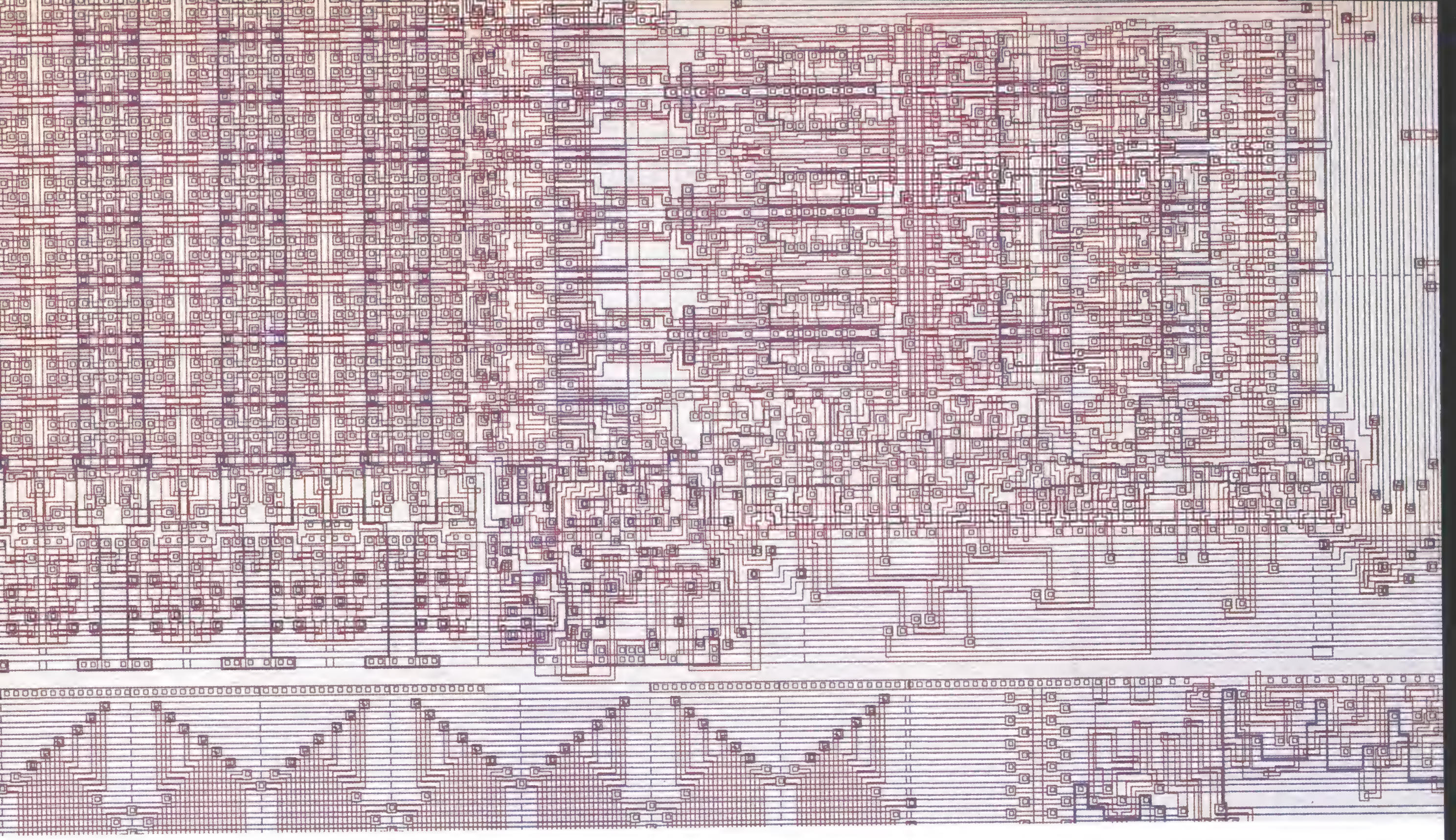
Circle No 362



MOTOR DRIVER

- *10 microsteps per step*
- *External resistor programs output current*

The MD10 bipolar stepping motor driver moves a 200-step hybrid PM motor at 2000 steps/revolution. The device eliminates low-speed resonance, according to the manufactur-



CALCOMP'S RESOLUTIONARY ADVANCE IN ELECTROSTATIC COLOR PLOTTERS.

Vivid color comes to high resolution electrostatic plotters.

CalComp introduces its new 5800 Series. Resolution is up to four times that of any other color electrostatic plotter—an incredibly sharp 160,000 dots-per-square-inch. The result is better definition, sharper lines and a smoother transition of colors.

Unlike other electrostatic plotters, the 5800 Series features random vector input. This eliminates the need for add-on controllers that take up extra space. And the 5800 provides internal rasterization and color separation to offload the host computer and increase plot throughput.

Registration is unmatched. Our patented electronic system registers each pass without any mechanical adjustment. Simply, there are no moving parts so you are assured of a new standard in accuracy and reliability.

And your maintenance will be minimal due to CalComp's exclusive Enviroclean™ toning system. Extensive diagnostics are built right in. And each plotter is backed by CalComp's worldwide field service network.

For a closer look at these resolutionary plotters, write CalComp, P.O. Box 3250, Anaheim, CA 92803. Or call 1-800-CALCOMP.

CALCOMP
A Sanders Company

CIRCLE NO 146

er. It can operate a range of 2-phase motors from a single-stack, 23-frame size to a multistack, 42-frame size with current ratings between 1.5 and 7.2A/phase. You can program the output current via an external resistor in a PWM circuit that uses power MOSFETs. The power-supply voltage range is 24 to 60V. The driver comes in a 4×4×1-in. package and requires no heat sink under most operating conditions. $350.

Oregon Micro Systems Inc, 15075 NW Pioneer Rd, Beaverton, OR 97006. Phone (503) 644-4999.

Circle No 363

SWITCH

- *Measures 0.295×0.098×0.197 in.*
- *Printed-circuit board terminals can be straight or right angle*

The AV4 Series snap-action switch measures 0.295×0.098×0.197 in. and weighs 0.007 oz. The device has gold- or silver-plated stainless-steel contacts and can be mounted on a pc board. Rigid pc-board terminals with both straight and right angles are available. You can also order integrally molded antiflux and solder-sealed terminals. Furthermore, you can specify that actuators be pin plunger, hinge lever, or simulated roller lever. $0.65 (1000). Delivery, six weeks ARO.

Aromat Corp, 250 Sheffield St, Mountainside, NJ 07092. Phone (201) 232-4260. TWX 710-997-9536.

Circle No 364

S/H AMPLIFIER

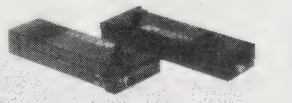
- *Has acquisition time of 40 nsec max*
- *Sample-mode bandwidth of 40 MHz*

The SHM-40 10-bit sample/hold amplifier features a maximum acquisition time (to 0.1% for a 2V step) of 40 nsec over the rated temperature range. The sample-mode bandwidth is 40 MHz. The unit contains an input buffer amplifier, an analog switch, a hold capacitor, and two output amplifiers, which can operate in parallel to reduce output impedance and double the output current. The device also specs a hold-mode droop of 100 μV/μsec. No adjustments are necessary. Feedthrough is −60 dB max over the temperature range. The amplifier is housed in a 24-pin, hermetically sealed, ceramic package and is available in three operating ranges. For 0 to 70°C range (SHM-40MC), $152; −25 to +85°C (SHM-40MR), $161; and −55 to +125°C (SHM-40MM), $171.

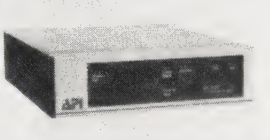
Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-9341. TWX 710-346-1953.

Circle No 365

from American Photonics:
the very latest & best in fiber optic products for your
Networking

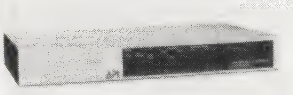


TR2000
Limited-Distance Modem (RS-232-C)
...an electro-optical replacement for RS-232-C null modem cables and DTE-to-DCE cables...full- and half-duplex operation.

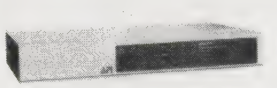


DL1120
Limited-Distance Modem (High-Performance, T-Carrier)
...for transmission of T-1, T-1C or T-2 data on multimode or single-mode optical fiber.

DL3500
Limited Distance Modem (High-Performance, V.35 Wire/Optical)
...a true modem emulator for V.35/RS-422 signals...can be used as either fiber or wire link...sync-data rates to 2.048 Mbps; async data rates from 0 to 300 kbps.



AFM2320
Multiplexer (RS-232-C, with 8 Asynchronous Channels)
...has both fiber optic and T-1 wire outputs...8 asynchronous channels with 3 lines each...async or sync data.



AFM7000
Multiplexer (Sync/Async, with 4 Sync Channels)
...offers high-speed fiber optic time division multiplexing...up to 16 async RS-232-C data channels or up to 4 sync RS-232-C or 4 V.35 channels, all at 76.8 kbps.

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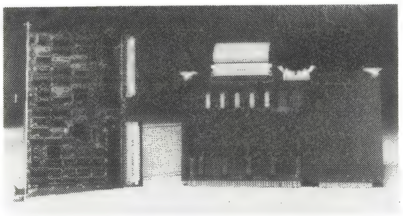
American Photonics Inc.
71 Commerce Drive, Brookfield Center, CT 06805
(203) 775-8950/8955 TELEX: 821353
Call TOLL FREE: 800-626-5745
CIRCLE NO 147



MULTIBUS INTERFACE

- *Links boards to the VME Bus*
- *Allows independent operation*

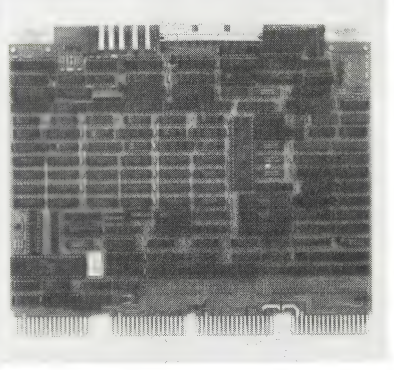
The Synergist Multibus/VME Bus board set provides signal and timing conversions that let you link VME Bus and Multibus I computer systems. Because the boards' operations are transparent to each bus, the computer on each bus can act either as a master or as a slave. Each computer can also disconnect itself from the bus-linking arrangement and operate independently. The boards support either 20- or 24-bit Multibus I addresses, and 24-bit VME Bus addresses. The bus-interconnection circuits furnish seven priority interrupts for both VME Bus and Multibus I computers. $1495.

HVE Engineering Inc, 1684 Dell Ave, Campbell, CA 95008. Phone (408) 370-4666.

Circle No 366

GRAPHICS CONTROLLER

- *Displays 16 million colors simultaneously*
- *Operates with Unibus and Q Bus computers*



Available as a quad-height board for DEC Q Bus or Unibus computers, the VCX-Q/U board creates color graphics images that can contain an independent alphanumeric overlay plane. The color display plane measures 256×256 pixels, and each pixel's color is set by a 24-bit value. An independent 8-bit look-up table for each color—red, green, and blue —lets you control as many as 16

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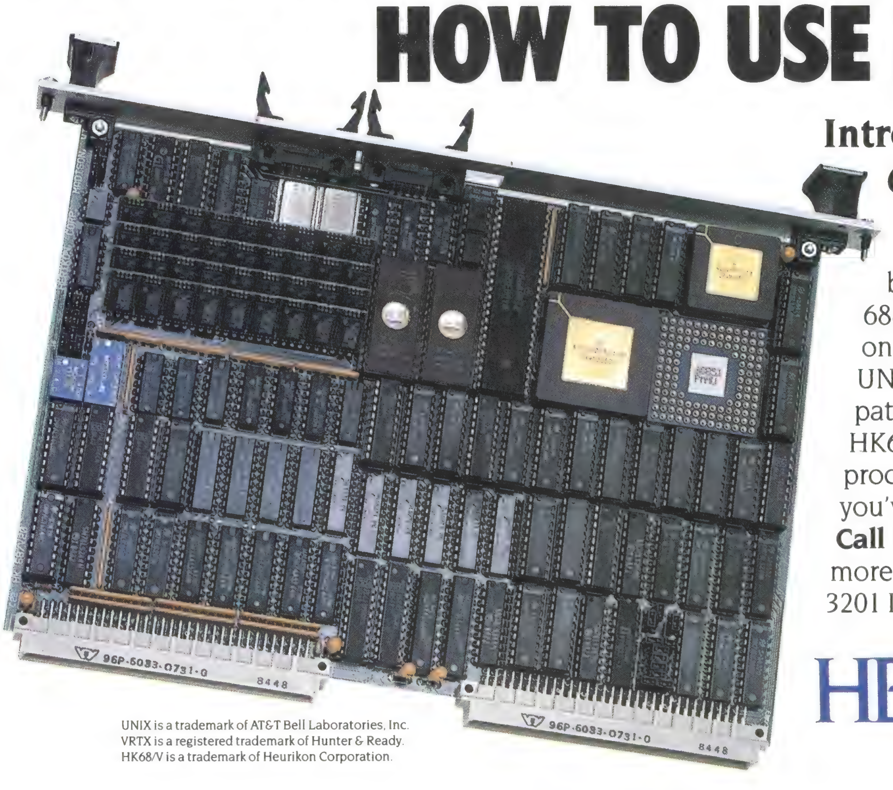

Introducing the HK68/V20 68020 VME processor.

Features include the 68020 MPU, 1 to 4 MegaBytes of on-board DRAM, 68851 PMMU, 68881 Floating Point Coprocessor, one serial port and MVMX/32. UNIX™ and VRTX® supported. Compatible with other members of the HK68/V™ Family of Heurikon VME processors. And technical support you've come to depend on.

Call 1-800-356-9602, Ext. 395 for more information. Heurikon Corporation, 3201 Latham Drive, Madison, WI 53713.

HEURIKON CORP.

UNIX is a trademark of AT&T Bell Laboratories, Inc.
VRTX is a registered trademark of Hunter & Ready.
HK68/V is a trademark of Heurikon Corporation.

CIRCLE NO 148

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perience**—Since we
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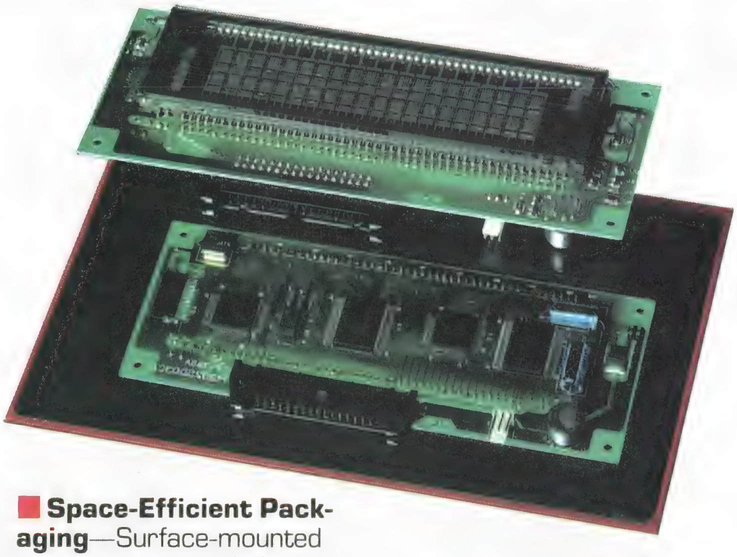
y and the module, our
perience in circuit design,
ftware, board assembly
d packaging enables us to
ck our products with in-
pth, knowledgeable
rvice.

Competitive Pricing—
Futaba, turnkey design
d production of our VF
odules eliminate a second
anufacturer's cost to you.
taba display modules are
ry price-competitive, as a
sult, making them more
asible for many applica-
ns which were not pre-
usly cost-effective.

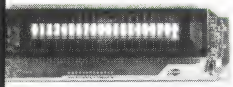
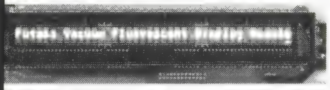
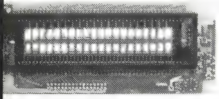
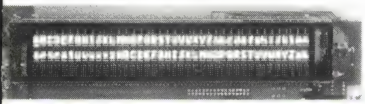


- **Space-Efficient Packaging**—Surface-mounted components, coupled with proven Futaba assembly know-how, result in a very space-efficient unit for your design.

- **Easy User Interfacing**—Only a 5 VDC power supply is required for these products. Users will also appreciate having both parallel and serial data input ports already on-board.

- **Long Unit Life with High Reliability**—Fewer components on-board and surface-mounting decrease the service requirements for Futaba modules, while increasing unit life with high performance reliability.

PLUS...you get the inherent benefits of vacuum fluorescent technology...high brightness, high contrast, superior readability and excellent viewing angle.

tandard Modules Available:		Sizes (Lines x Characters)	Character Size	Module Dimensions
	**M20SD01CA**	**1 x 20**	**.20″**	**6.3″ x 1.97″ x .75″**
	M20SD42CA	**1 x 20**	**.344″**	**7.1″ x 2.16″ x .88″**
	**M40SD02CA**	**1 x 40**	**.20″**	**9.45″x 2.16″ x .88″**
	M40SD42CA	**1 x 40**	**.344″**	**9.45″x 2.16″ x .88″**
	**M202SD03CA**	**2 x 20**	**.20″**	**6.7″ x 2.56″ x .90″**
	**M402SD04CA**	**2 x 40**	**.20″**	**10.43″x 2.56″ x .90″**

■ ■

For state-of-the-art display modules, industry knows only one name,
Futaba Corporation of America.
Please contact Futaba directly at 312-884-1444
or your local Futaba representative:

FUTABA
Corporation of America
Electronic Components Division

Futaba Corporation ■ 711 East State Parkway ■ Schaumburg, IL 60195
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CIRCLE NO 149

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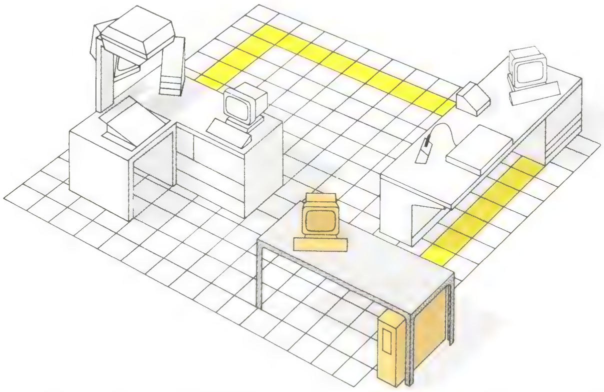

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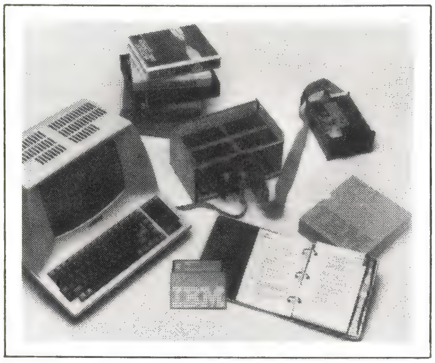
CIRCLE NO 152

million colors at any time. The independent alphanumeric display supplies a 50-line display of 80 characters/line. You can choose among 64 character colors and 64 background colors. The board furnishes an RS-330-compatible output of separate or mixed graphics- and alphanumeric-display signals. The manufacturer supplies test routines, initialization routines, and a subroutine library for both C and Fortran. $5895. Delivery, 45 days ARO.

Peritek Corp, 5550 Redwood Rd, Oakland, CA 94619. Phone (415) 531-6500.

Circle No 367

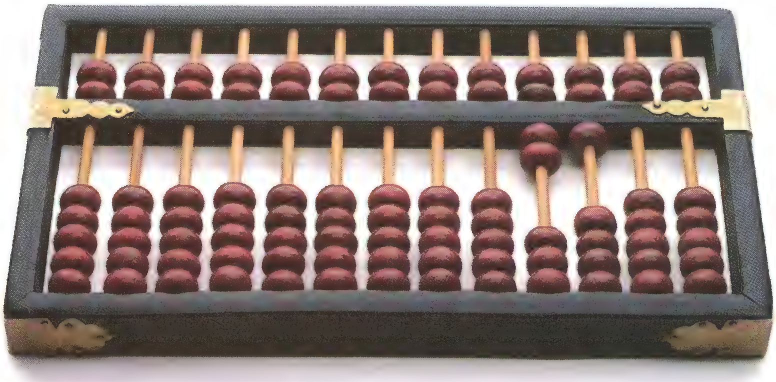


STD BUS CPU

- *Runs PC-DOS software*
- *Drives STD Bus peripherals*

By using the DOS088-54 package, designers can implement PC-DOS and MS-DOS software in STD Bus computers. The system includes three STD Bus cards, a set of BIOS (basic I/O system) routines in EPROM, and PC DOS software on a 5¼-in. disk. The disk drives read and write information in IBM-PC-type format so you can exchange disks with an IBM PC or a compatible computer. The CPU includes 128k bytes of memory, an RS-232C I/O port, a parallel printer port, and interface circuits for two floppy-disk drives. The BIOS software supports extra serial I/O cards and lets you control the serial ports as COM1 or COM2 devices. Cables provide connections to an RS-232C-compatible terminal, a parallel printer, and a

Continued on pg 259



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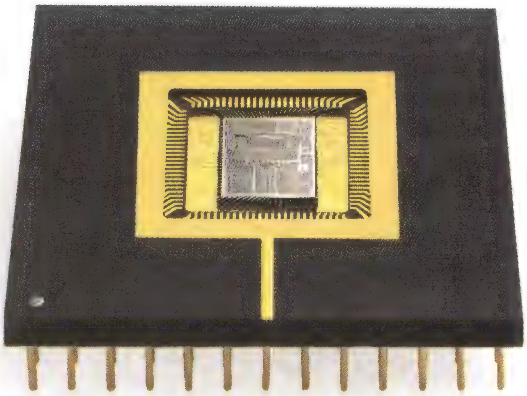

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2V	200A
5V	150A
12V	70A
15V	55A
24V	35A
28V	28A
48V	17A

1000 WATT — JF101 — 5″x 8″x 11″

OUTPUT VOLTS	AMPS @50°C
5V	200A
12V	83A
15V	67A
24V	43A
28V	37A
48V	21A

1500 WATT — JF1500 — 5″x 8″x 13.5″

OUTPUT VOLTS	AMPS @50°C
2V	300A
5V	300A
12V	125A
15V	105A
24V	65A
28V	55A
48V	32A

acdc electronics

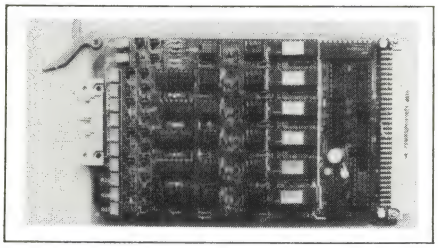
401 JONES ROAD, OCEANSIDE CA 92054 TEL: 619/757-1880. TWX: 910-322-1470.

CIRCLE NO 157

5¼-in. floppy-disk drive. The computer system is compatible with STD Bus peripheral cards. $1450.

Micro/sys Inc, 1011 Grand Central Ave, Glendale, CA 91201. Phone (818) 244-4600.

Circle No 368



CONVERTER MODULE

- *Offers six D/A outputs*
- *Runs on RM 65 Bus*

The RM65-5306E, a D/A-converter module, has six independent channels of analog output and specs 12-bit resolution. Measuring 100×160 mm, the module is Eurocard size and is compatible with the RM 65 Bus. It requires ±5V and ±15V supplies. An internal reference voltage lets you select one of four output-voltage ranges—0 to 5V, 0 to 10V, ±5V, or ±10V—for each D/A output channel. You can establish additional output ranges by supplying two external reference voltages, each of which controls three channels. Two potentiometers for each channel calibrate output offset and gain. Output slew is 10V/μsec, and settling time is 10 μsec. $450.

Dynatem Inc, 19 Thomas, Irvine, CA 92718. Phone (714) 855-3235. TWX 910-595-2603.

Circle No 369

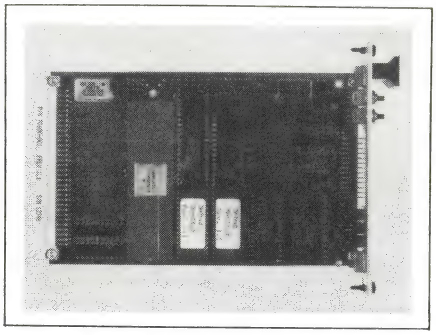
IBM PC LINK

- *Controls Multibus systems*
- *Supports DMA transfers*

The PC/796 Link connects the IBM PC to Multibus computers and I/O boards via two circuit boards connected by a ribbon cable. One board is installed in the PC, and the other is located in any Multibus enclosure. The PC and the Multibus can be as much as 50 ft apart and they can be optically isolated. This link enables the PC to act as a Multibus controller with access to Multibus address space. You can configure the PC as a Multibus master or share the Multibus with other Multibus processors. You can also transfer data between the PC and the Multibus system via the PC's DMA controller. $725.

Ultralink, 1091 Airport Rd, Minden, NV 89423. Phone (702) 782-9758.

Circle No 370



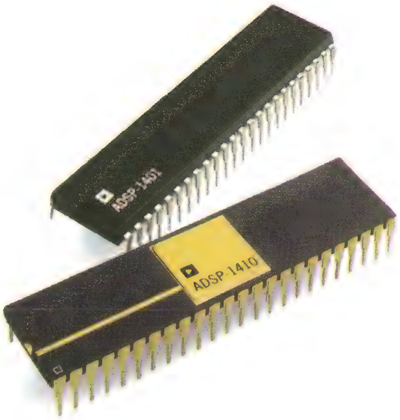
VME CPU

- *Provides a 10-MHz 68000 or a 68010 μP chip*
- *Contains six byte-wide memory sockets*

The single-height XVME-600 VME Bus CPU module provides either a 10-MHz 68000 or a 68010 μP chip, both of which operate with no wait states when programs are available in onboard memory. The board contains six byte-wide memory sockets, two for EPROMs and four for static RAMs. The sockets let you supply as much as 128k bytes of RAM and a 128k-byte EPROM for the computer. The board also furnishes two RS-232C serial ports and a 16-bit timer. The RS-232C signals are available at a connector on the front of the board. The board operates as an A24:D16 VME Bus master, and it handles interrupts 0 through 7. $600.

Xycom Inc, 750 N Maple Rd, Saline, MI 48176. Phone (313) 429-4971.

Circle No 371



THE COMPLETE SOLUTION FOR MICROCODED PROCESSORS.

Analog Devices' ADSP-1401 and ADSP-1410 offer you the highest speed and the greatest functionality for key tasks in microcoded systems – microprogram sequencing and data address generation.

The ADSP-1401 MicroProgram Sequencer is the industry's most advanced IC for generating microcode addresses. It supplies 16-bit addresses with a clock-to-address delay of just 25ns. The chip supports 10 maskable, prioritized interrupts, as well as traps. A 64-word internal RAM is user-configurable for subroutine stack, register stack, and parameter storage. Four event counters streamline nested loops.

The ADSP-1410 is the industry's only IC dedicated to flexible, high-speed data address generation. It provides 16-bit pointers to data memory 30ns after the clock edge. Its thirty registers hold address pointers, offsets, comparison values, and initialization values. With its powerful zero-overhead looping structure, the device can – in a single cycle – output an address, modify it, and conditionally branch to an initialization address.

Both Word-Slice™ components offer low-power CMOS technology (≤ 375 mW) in a 48-pin ceramic or plastic DIP. And, microcode system development tools and support are available from many third parties, including Hewlett-Packard, Step Engineering, and HiLevel Technology.

For more details, call your nearest Analog Devices, Inc. Sales Office.

ANALOG DEVICES

CIRCLE NO 153

What company could offer this broad range of EnduraLine™ non-metallics?

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When it comes to offering non-metallic enclosures designed to survive in corrosive environments, we've been in business a long, long time. First, with fiberglass. Next, with polyester and ABS. Now, with new tough polycarbonate.

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Hoffman EnduraLine non-metallic enclosures conform to such specifications as NEMA Type 4, Type 4X, Type 12 and Type 13 standards as well as European standards IEC 529-IP64, IP65, IP66 and IP67.

EnduraLine enclosures are just part of more than 2,500 models Hoffman carries in standard inventory. This vast selection is one reason why specifiers designate Hoffman enclosures as their primary choice.

For complete information and specifications on EnduraLine™ non-metallic enclosures, contact your Hoffman representative.

Your informed source

CIRCLE NO 158

Hoffman®

HOFFMAN ENGINEERING COMPANY
Division of Federal Cartridge Corporation
Anoka, Minnesota 55303. (612) 421-2240
Dept. EDN-859

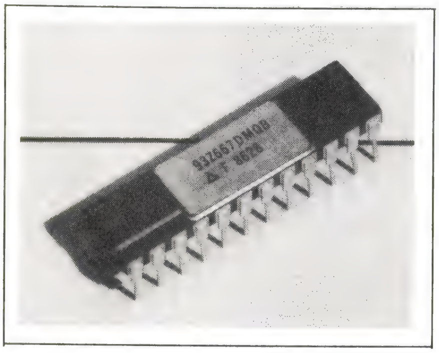
STATIC RAMs

- *Feature 24- and 35-nsec access versions*
- *JEDEC-standard pinout*

The MCM6268, -6287, and -6288 static RAMs are organized as 4k×4 bits, 64k×1 bits, and 16k×2 bits, respectively. According to the manufacturer, these are the first production RAMs to use a double-metal, double-polysilicon CMOS process in conjunction with 1.5-μm design. Each device comes in 25- and 35-nsec access-time versions. Their circuit architecture helps give them both high speed and low active power. The devices have JEDEC-standard pinout. In 300-mil, 20-pin plastic DIPs, the 6268P25 and -35 cost $16.80 and $11.20; in 300-mil sidebrazed packages, the -6287L25 and -35 cost $43.40 and $35. Models -6288L25 and -35 are $54.60 and $42 (100).

Motorola Inc, Box 52073, Phoenix, AZ 85072. Phone (512) 928-6707.

Circle No 372



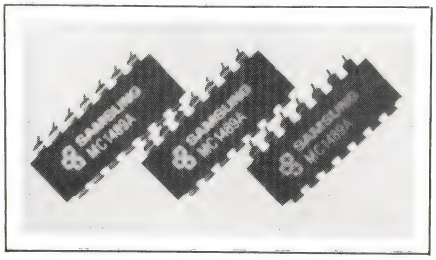
64k-BYTE PROM

- *Features 3-state output*
- *Memory expansion to 128k bytes*

The 93Z667 TTL bipolar PROM, organized as 8192×8 bits, features an access time of 40 nsec. It's adapted for applications such as telecommunication systems that require advanced packet-switching data rates of 64k to 2M bps. The device has 3-state outputs that provide active pullups when enabled and high output impedance when disabled. Thus, the outputs allow optimal word expansion in bus-organized systems. One chip-select input is available for logic flexibility and for memory-array expansion to 128k bytes without external decoding; the fast chip-select access time permits direct address decoding without increasing overall memory-access times. $57.15 (100).

Fairchild Semiconductor, Memory and High Speed Logic Div, 1111 39th Ave SE, Puyallup, WA 98373. Phone (800) 554-4443.

Circle No 373



RS-232C ICs

- *Interface system between DTL or TTL logic levels*
- *Turn-on voltage of 1.95V*

The MC1488 quad driver and its companion MC1489A quad receiver provide an interface system between DTL or TTL logic levels and RS-232C defined levels. The -1489A device specs a turn-on voltage of 1.95V, a turn-off voltage of 0.8V, and a hysteresis voltage of 1.15V. The driver and receiver are intended for use in modems, add-on memory boards, printers, plotters, and any data-communications system. $0.35 (100).

Samsung Semiconductor, 5150 Great America Parkway, Santa Clara, CA 95054. Phone (408) 980-1630. TLX 339544.

Circle No 374

FLOATING-POINT CHIP SET WITHOUT COMPROMISE.

Analog Devices' ADSP-3210/3220 floating-point multiplier and ALU are the industry's best available solution for fast IEEE arithmetic. This chip set provides blazing throughput and low latency – without compromise.

The chips execute an extensive set of operations on 32- and 64-bit IEEE floating-point and 32-bit fixed point. So, systems using them have the flexibility to support all standard data formats.

Circuit innovations and a fast 1.5μm process allow each chip to achieve 10 MFLOPS for most operations. And with CMOS, there are no power or reliability penalties.

What's more, number-crunching speed doesn't come from cumbersome pipelining. Because it has just one internal pipeline stage, the ADSP-3210/3220 is the industry's lowest-latency double precision chip set in production. And, with this architecture, microcode development is simple.

For more details, call your nearest Analog Devices, Inc. Sales Office.

ANALOG DEVICES

CIRCLE NO 154

We proudly introduce our MetaICE™-80515, the industry's first cost-effective, PC-hosted in-circuit emulator for Siemens Components' new 80515 high-integration single-chip microcontroller.

The 80515 microcontroller is one of the first proliferation devices developed for the MCS™-51 microcomputer family. Naturally, MetaLink™ delivers you full hardware and software emulation support. And our MetaICE-80515 comes standard with all the MetaLink features and options that you've come to rely on with our emulators.

Adding the MetaICE-80515 to our line demonstrates our continuing commitment to the ever expanding MCS-51 microcomputer family. A commitment that began with the introduction of our emulators for the 8031, 8032, and 8344 devices and grew with the addition of emulators for the 8051, 8052 and 8044 devices. A commitment that will continue to grow as the MCS-51 microcomputer family expands.

This commitment has seen MetaLink emerge as the technical leader in providing cost-effective, PC-hosted emulation support for the MCS-51 microcomputer family. Recognized as the leader in giving you the best software and hardware — and the easiest to use — for your money.

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CIRCLE NO 159

BOOSTER IC

- *Capable of ±1V output into a 100Ω load*
- *Replacement for Harris's Model HA3-5033-5*

The AH001 video current booster is a pin-for-pin replacement for Harris's (Melbourne, FL) Model HA3-5033-5. You can use the device in a range of applications from S/H circuits to A/D and D/A converters. The device specifies a minimum output current of ±100 mA in a 100Ω load at a typical output frequency of 24 MHz. It's capable of ±1V output into a 100Ω load to 39 MHz. $5.70 (100).

Optical Electronics Inc, Box 11140, Tucson, AZ 85734. Phone (602) 624-8358. TLX 283347.

Circle No 375

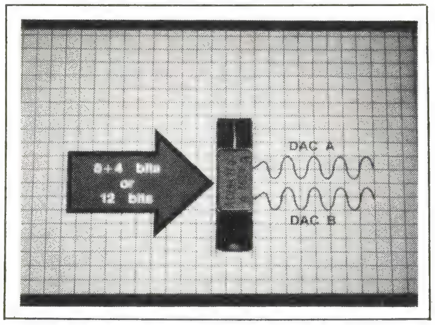
MODEM IC

- *Contains on-chip automatic gain control*
- *Dynamic range of 70 dB*

The MSM6950 modem front end contains an on-chip automatic-gain-control (AGC) circuit. You can control the AGC externally using an 8-bit digital signal. The device has a received-signal-level range of 48 dB with 0.19-dB steps. The unit features a voltage-gain range of −4 to +43.8 dB and voltage-gain accuracy of ±0.4 dB. It contains an A/D converter with 8-bit parallel outputs and a D/A converter with 8-bit parallel inputs. The IC has a dynamic range of 70 dB. It can communicate with a modulator and a demodulator via each of the 8-bit parallel digital lines. It requires a 3.6864-MHz clock rate to generate the necessary operating time base, and it works from supply voltages of ±5V. In 42- and 56-pin plastic leaded chip carriers, $15 (100).

Oki Semiconductor, 650 N Mary Ave, Sunnyvale, CA 94086. Phone (800) 336-3555; in CA, (408) 720-1900. TWX 910-338-0508.

Circle No 376



D/A CONVERTERS

- *Each chip contains two 12-bit DACs*
- *Data registers and control logic are on chip*

The AD7537 and -7547 are dual D/A-converter chips. Each chip contains two 12-bit current-output DACs and features a different output bus structure. Also on chip are data registers and control logic for easy μP interfacing. The dual DAC construction occupies half the area required by two separate 12-bit DACs; it also allows ladder-resistance matching of 0.5% and precise tracking between the DACs. The -7547 features a 12-bit parallel-loading structure that allows you to load data in one 12-bit word. The -7537 offers a 2-byte input structure for right-justified loading from an 8-bit bus. Both devices feature 4-quadrant multiplication. In 24-pin plastic or hermetically sealed DIPs, the AD7537JN and AD7547JN cost $14.50 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565.

Circle No 377

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ANALOG DEVICES

CIRCLE NO 155

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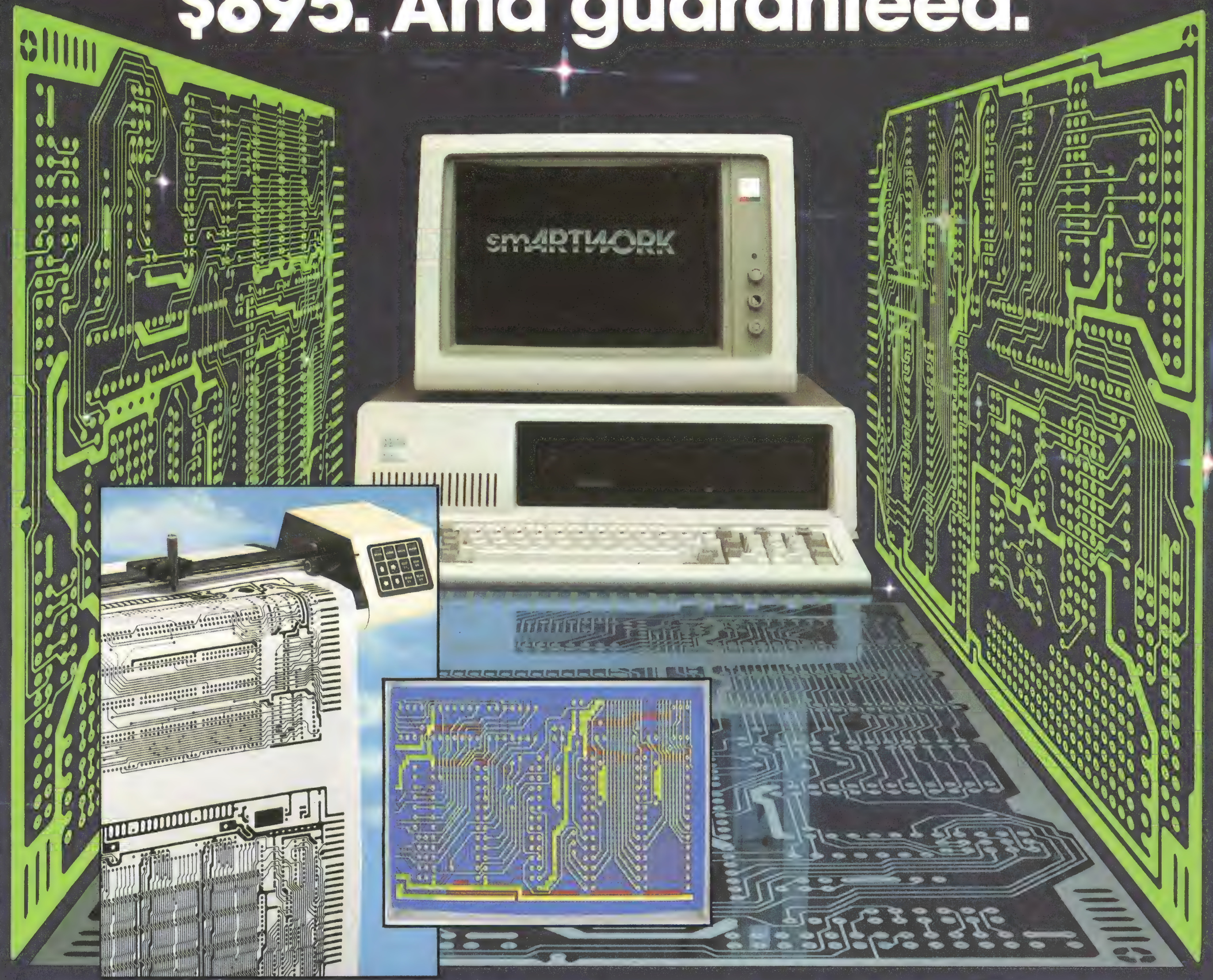

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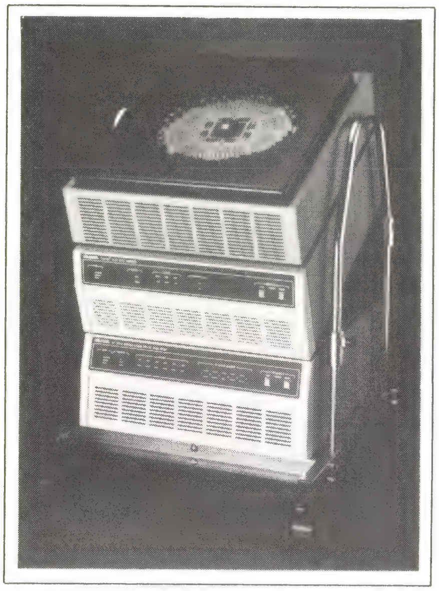


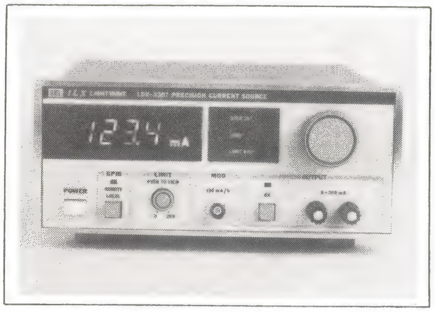
VLSI VERIFIERS

- *Feature 500-psec timing resolution*
- *Support VLSI devices having as many as 512 pins*

The Topaz prototype VLSI-device verification system comes in two versions: the Topaz-50 and the Topaz-25. The models operate at 50 and 25 MHz, respectively. Both support VLSI devices having as many as 512 pins. The systems feature programmable drivers and receivers on each pin, 500-psec timing resolution, automatic signal-edge deskewing, a logic analyzer, and software links to most CAE simulation programs. Plug-in options for the systems include 4k-, 16k-, and 64k-byte vector memories in 16-pin increments. Each plug-in has 16 I/O pins and provides two independently controlled strobe pins; you can program the timing and format of the I/O pins in 8-pin segments. The pin drivers allow for programmable high and low levels from −3 to +7V with 10-mV resolution. The drivers supply 30-mA drive currents into both ECL and CMOS loads. The receivers allow you to program the threshold over a ±10V range with 10-mV resolution; they feature 1-MΩ input impedance. The entire system has less than 35-pF loading on device output pins. As many as four optically isolated power supplies allow you to program the power to the device under test over a ±7V range and to program the current from 0 to 5A. The systems come with IBM PC/AT software and three of the company's software programs: Wave-Gen, Meta-Shmoo, and EPL. 25-MHz system, $34,000; 50-MHz system, $230,000. Delivery, 60 to 90 days ARO.

Hilevel Technology Inc, 18902 Bardeen, Irvine, CA 92715. Phone (800) 445-3835; in CA, (800) 752-5215. TLX 655316.

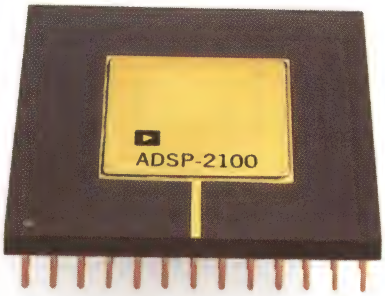
Circle No 378



LASER SOURCE

- *IEEE-488 compatible*
- *Transient-free power up and power down*

You can use the LDX-3207 precision current source for semiconductor laser diodes and other transient-sensitive devices. The current source supplies 0 to 200 mA and has a compliance voltage of 5V; it maintains a transient-free output under all operating conditions. The output is stable to better than 100 ppm/°C; its noise and ripple are typically less than 10 mA rms at a 100-mA nominal output. An adjustable, front-panel current-limit control and an output shorting circuit that's active during power-up and power drop-



BREAKTHROUGH PERFORMANCE FROM A DSP MICROPROCESSOR.

Analog Devices' ADSP-2100 is the first single-chip DSP microprocessor to break the bit-slice performance barrier. Now, for the first time, high-performance and ease-of-design are combined in a single CMOS DSP solution.

For calculation-intensive algorithms, the 2100 features three independent computational units: a 16-bit ALU, a 16 x 16 multiplier with a 40-bit accumulator and a robust barrel shifter. To keep the numbers coming, the 8 MIPS processor has unmatched program sequencing and data address generation capabilities.

The ADSP-2100's architecture allows two operands to be fetched from off-chip in parallel with on-chip computation. With this efficient use of external memory (up to 48K) you'll avoid the I/O bottlenecks typical of other processors.

Extensive ADSP-2100 support streamlines your development schedule. The processor is programmed in a high-level algebraic assembly language. Development tools include extensive software support and a full-speed emulator.

Whether your application is modems, speech, imaging, graphics, radar, sonar, or control, the ADSP-2100 gives you outstanding performance, while speeding your project to completion.

For more details, call your nearest Analog Devices, Inc. Sales Office.

ANALOG DEVICES

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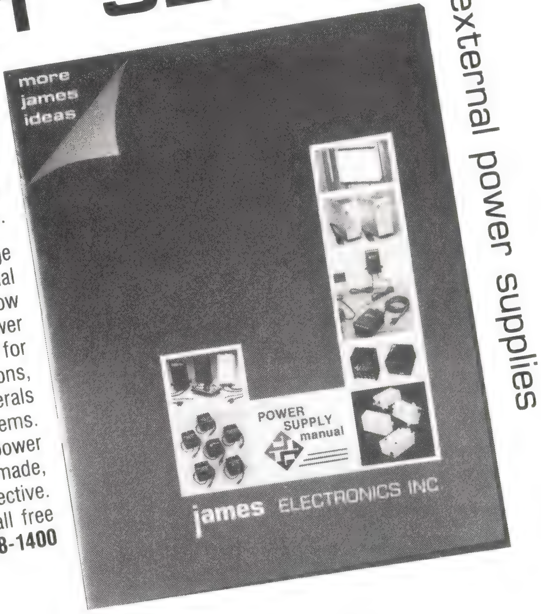

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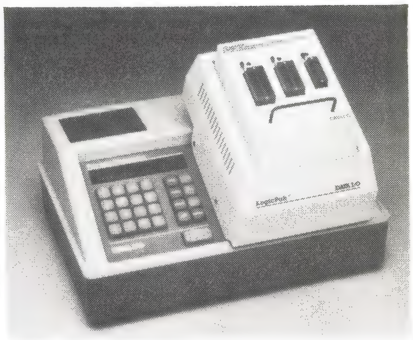
CIRCLE NO 162

outs provide output transient protection. This circuit also provides a means of output on/off switching with a soft-turn-on characteristic. You can control the current source in three ways: by using the main front-panel output-adjusting knob, by using a modulation/voltage programming input, or by using an optional IEEE-488 interface. LDX-3207, $1195. Model 1205 interface, $575.

ILX Lightwave Corp, Box 6310, Bozeman, MT 59715. Phone (406) 586-1244.

Circle No 379



PLD ADAPTERS

- *303A-011A replaces five adapters currently in use*
- *Handles PLCCs*

Model 303A-011A, a device-programmer adapter for the company's 29B device programmer suits PLDs in DIPs. It takes the place of five adapters currently in use. The second adapter, the 303A-011B, programs PLDs that come in surface-mount packages. The adapters perform continuity checks on each device pin before the part is programmed. By employing the 29B's 1M-byte RAM option, you can use nearly 10,000 vectors to test a device. DIP version, $895; PLCC version, $1195. Delivery, four weeks ARO for the DIP version, eight weeks ARO for the PLCC version.

Data I/O, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. TLX 152167.

Circle No 380

EDN REPRINTS

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CMOS ICs

As featured in EDN Magazine

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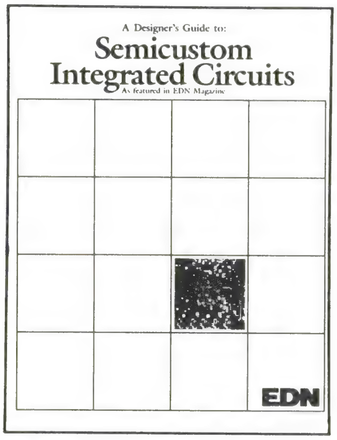

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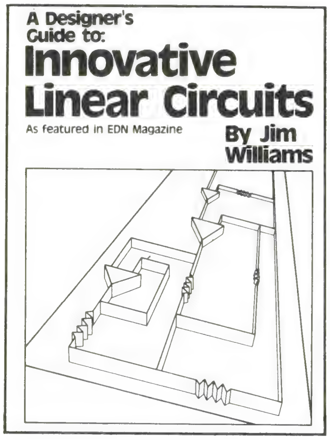

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By Jim Williams

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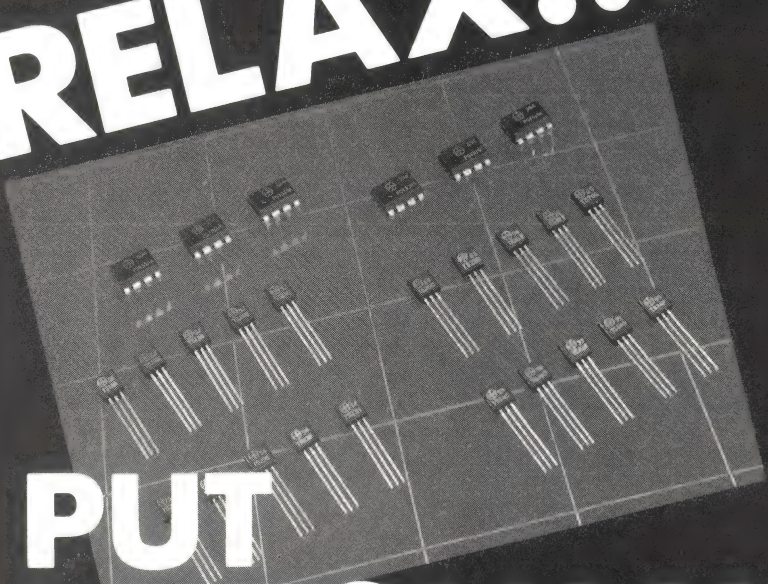

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CIRCLE NO 164

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INSTRUMENTATION & POWER SOURCES

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Yag-Drive is a power supply and laser controller that weighs 50 lbs and occupies a 7×19-in. rack. Available in either a 6- or 10-kW version, the device features a 50A output with an operating voltage range of 250V dc max. Ripple and noise are 0.2%, and regulation is better than 0.2%. Supply efficiency is over 90%. The unit requires 3-phase 208V ac input. Its rear-panel connector provides remote system control. $3300 to $3800. Delivery, 45 days ARO.

ALE Systems Inc, 150 Homer Ave, Ashland, MA 01721. Phone (617) 881-5252. TLX 928207.

Circle No 381

POCKET COMPUTER

- *Accepts Basic and assembler programs*
- *Peripherals available*

The PB-1000 pocket computer has an 8k- to 40k-byte memory. The device features a touch-sensitive LCD screen that displays 4 lines of 32 characters each. You can program the computer in Basic and assembly language. The computer has a built-in data bank. Options for the computer include an RS-232C interface, a Centronics output, a compact 80-column printer, a microfloppy-disk drive, a full-size color plotter, a cassette interface, and a communications interface.

Casio Inc, 15 Gardner Rd, Fairfield, NJ 07006. Phone (201) 575-7400.

Circle No 382

INTERNATIONAL

POWER DARLINGTONS

- *Devices switch 2.5 to 20A*
- *Fall time of <0.4 μsec*

Featuring a fall time of less than 0.4 μsec, the BUD Series of power Darlingtons includes versions that can switch between 2.5 and 20A at collector voltages below 450V. The devices have a current gain of 20 minutes. All the devices have an integral speed-up diode. The BUD 46 and BUD 47, rated at 2.5 and 5A, respectively, come in TO-220 cases; the BUD 48 and BUD 98, rated at 10 and 20A, respectively, are available in nonisolated or isolated TOP-3 packages. All these devices are available with either an 850V or a 1000V V_{CEV} rating. One version of the BUD 48, packaged in an isolated TOP-3 case and having a V_{CEV} rating of 600V, features an integral flywheel diode. BUD 46, $0.95; BUD 47, $1.50; BUD 48, $2.45; BUD 98, $5.00 (10,000).

Thomson Semiconductors, 45 ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 204780.

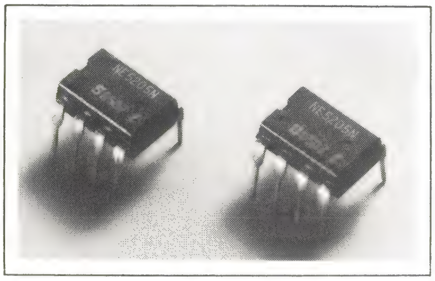
Circle No 383

Thomson Components, 7950 E Redfield Rd, Scottsdale, AZ 85260. Phone (602) 951-2900.

Circle No 384

WIDEBAND AMPLIFIER

- *Provides 20-dB gain from dc to 500 MHz*
- *Matches 50 or 75Ω source/load impedances*



The NE5205 wideband amplifier is a 4-terminal, fixed-gain, noninverting amplifier. It specs a 20-dB gain with a 3-dB bandwidth from dc to beyond 600 MHz. You can use the device with 50 or 75Ω sources and loads. VSWR on either the input or output is <1.5 over the entire bandwidth. The amplifier requires no components for external compensation. It operates from a single 6V supply and typically draws 25 mA. The device is available in an 8-pin SO package for surface mounting, in a 4-lead TO-46 metal case, and in a plastic or a ceramic package. In the TO-46 and plastic-DIP versions, the

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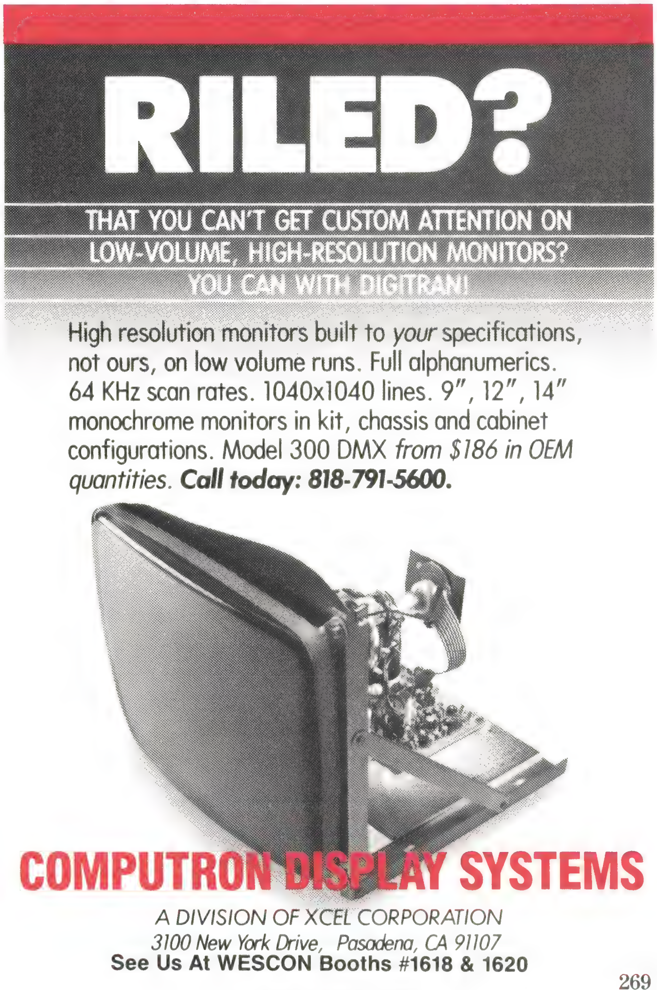
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device is available in versions for the military temperature range. The TO-46 version has a case grounding pin that allows you to extend the upper 3-dB point to 650 MHz. $2 (100).

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

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Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000.

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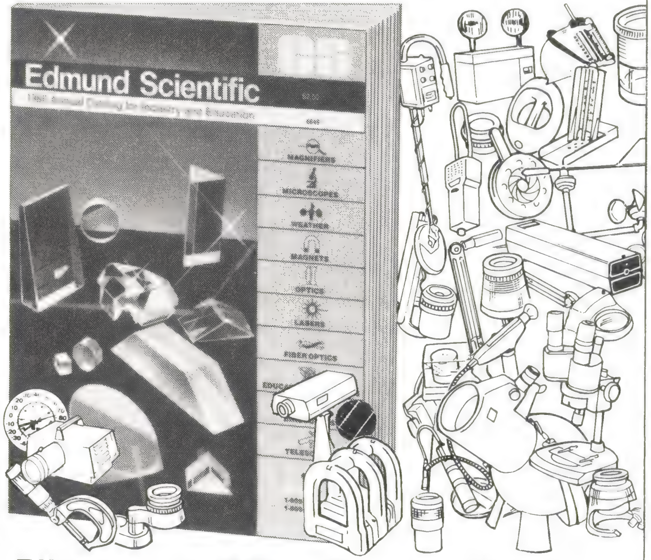

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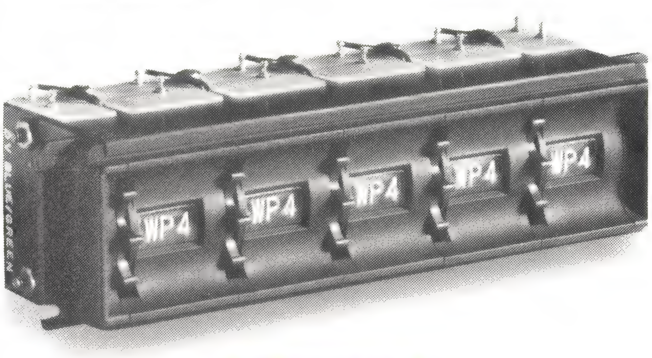

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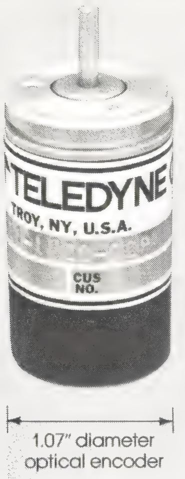

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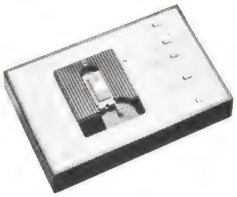

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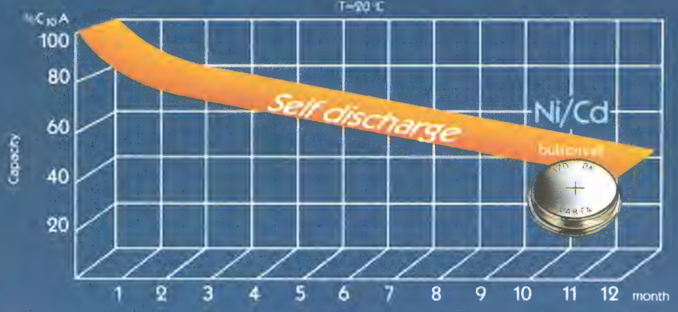

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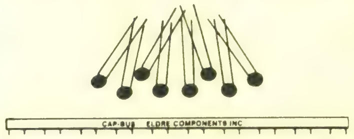

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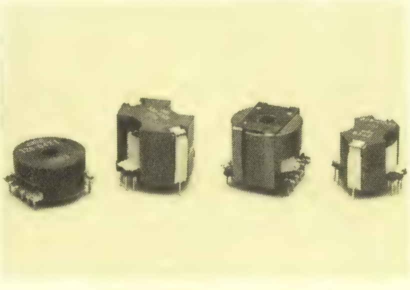

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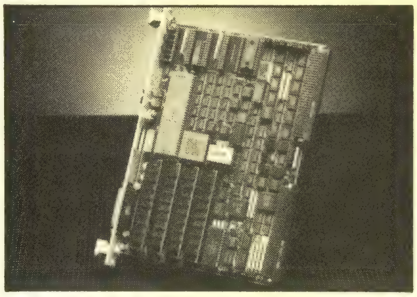

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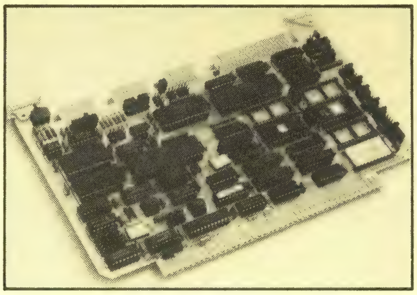

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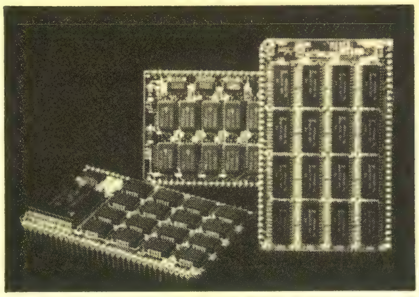

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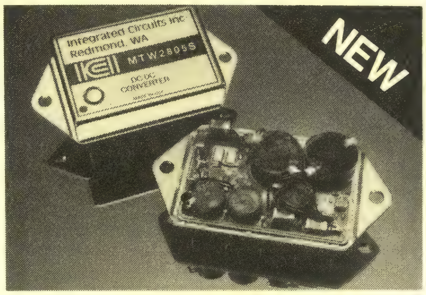

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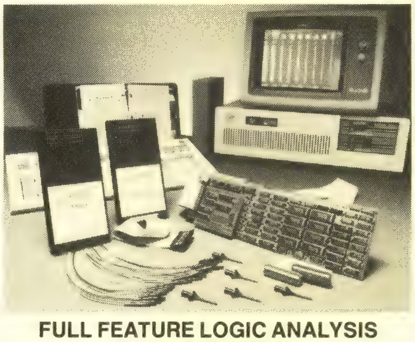

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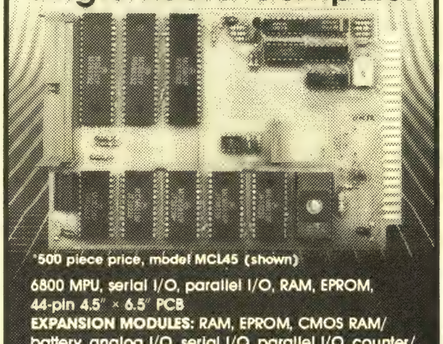

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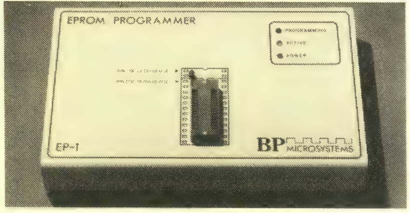

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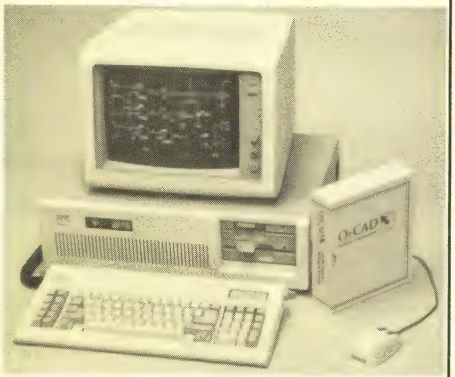

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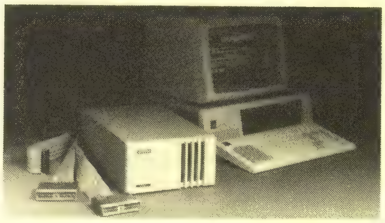

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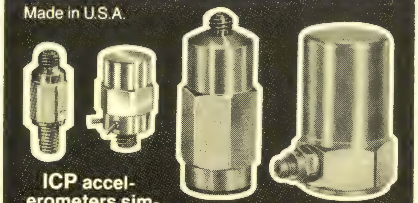

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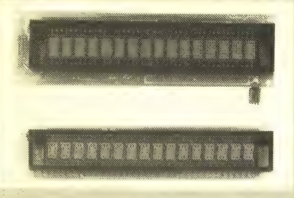

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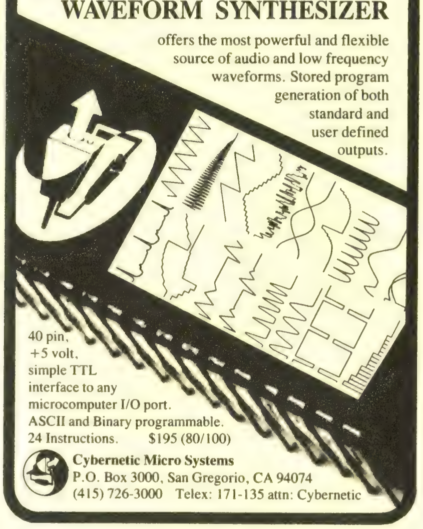

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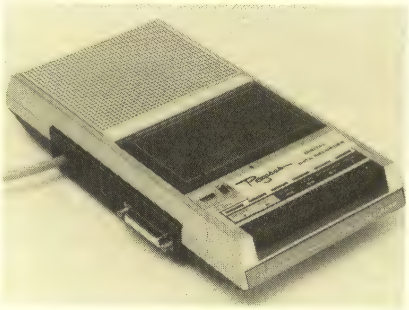

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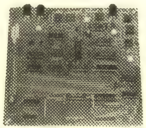

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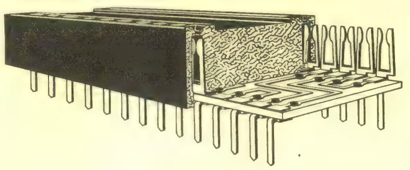

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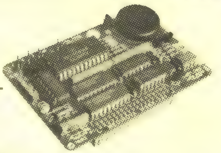

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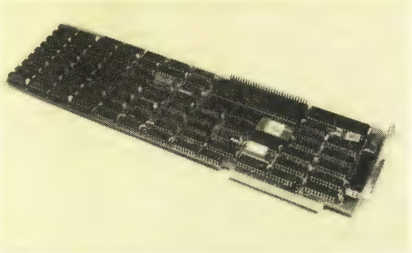

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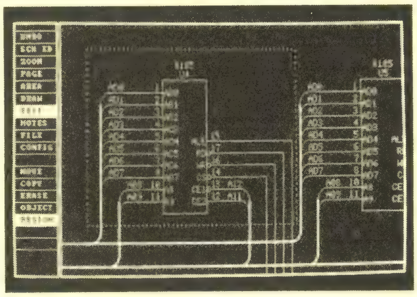

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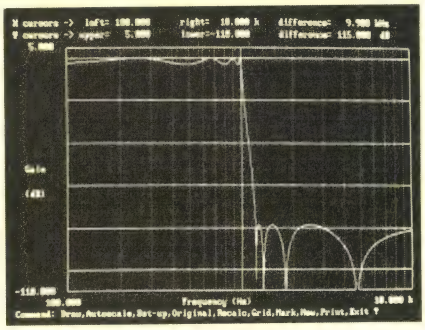
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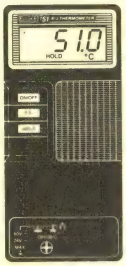

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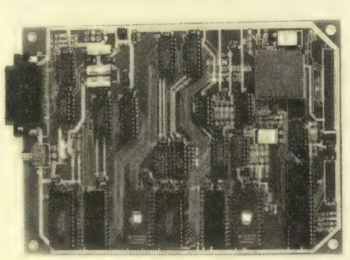

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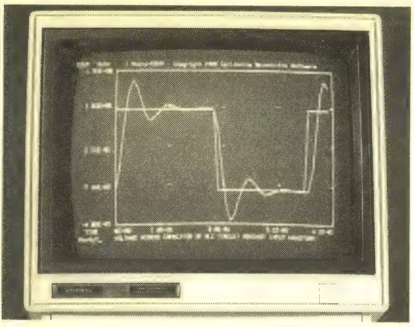

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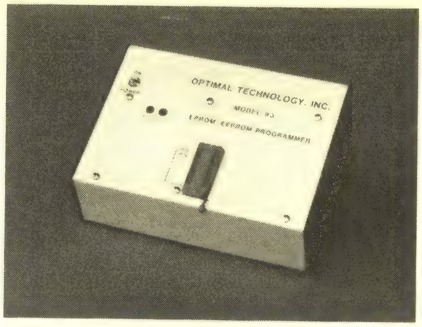

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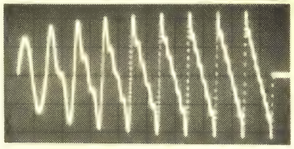

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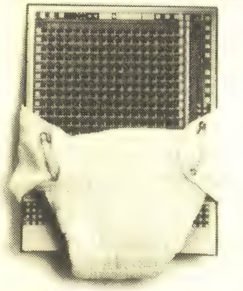

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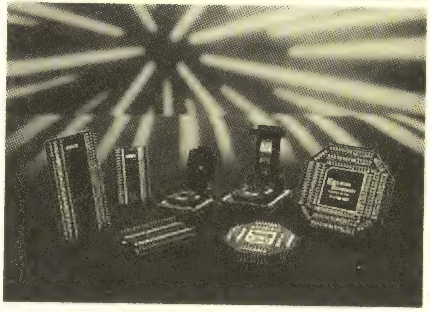

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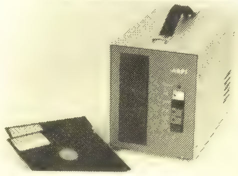

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Brochure depicts fiber-optic kit

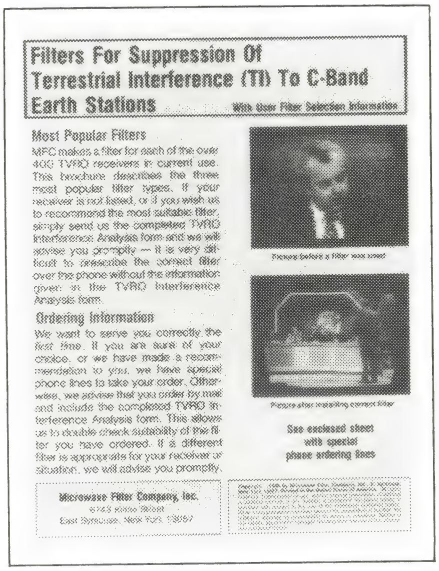
This 4-pg, 4-color brochure describes a fiber-optic, RS-232C modem hardware kit. The kit consists of two asynchronous modems and power sources, plus 100 ft of twin fiber-optic cable with assembled connectors. The brochure shows you how to install the device, and it also provides specifications and a parts list.

Augat Fiberoptics, 710 Narragansett Park Dr, Pawtucket, RI 02861.

Circle No 391

Pamphlet addresses terrestrial interference

This pamphlet describes the manufacturer's filters, which suppress terrestrial interference in more than 400 satellite receivers. The brochure concentrates on three filter lines that are used to solve most T1 problems, and it contains a list of receivers and filters compatible with the lines. In addition, it contains a TVRO-interference analysis form, which you can fill out and send in for a specific filter recommendation if a particular receiver isn't listed. Finally, the pamphlet includes information on how to identify interference.



Filters For Suppression Of Terrestrial Interference (TI) To C-Band Earth Stations

With User Filter Selection Information

Most Popular Filters

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Ordering Information

We want to serve you correctly the first time. If you are sure of your choice, or we have made a recommendation to you, we have special phone lines to take your order. Otherwise, we advise that you order by mail and include the completed TVRO Interference Analysis form. This allows us to double check suitability of the filter you have ordered. If a different filter is appropriate for your receiver or situation, we will advise you promptly.

Picture before a filter was used

Picture after installing correct filter

See enclosed sheet
with special
phone ordering lines

Microwave Filter Company, Inc.
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Microwave Filter Co Inc, 6743 Kinne St, East Syracuse, NY 13057.

Circle No 392

Slide chart determines amplifier performance

This slide chart enables you to ascertain critical amplifier parameters. After you provide the noise figure, bandwidth, and gain, the slide chart can determine third- and second-order intercept points and dynamic range. Moreover, you can use it to calculate 2-stage cascade intercepts and noise figures, and you can convert return loss to VSWR. Request on company letterhead.

Amplifonix Inc, 2010 Cabot Blvd W, Langhorne, PA 19047.

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This 36-pg directory of computer-security products lists descriptions of 93 vendors. Each directory entry includes company name, address, and phone number; contact name; and a paragraph describing the company's products or services. The catalog is free, but you must send a 9×12-in. self-addressed envelope with $1.24 postage affixed.

Computer Security Institute, 360 Church St, Northborough, MA 01532.

INQUIRE DIRECT

App note describes test criteria for hybrids

A 4-pg application note, *Understanding Quality Conformance Inspection of Hybrid Microcircuits,* describes the requirements you must fulfill to meet Test Method 5008 of MIL-STD-883. The note explains the tests necessary to meet the military specs, and a series of seven tables lists the tests.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

Circle No 395

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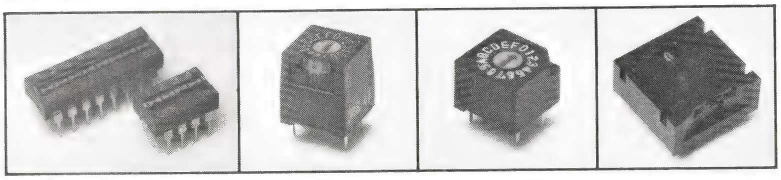

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CIRCLE NO 174

PROFESSIONAL ISSUES

Support organizations for inventors take the loneliness out of creating

Deborah Asbrand, *Staff Editor*

It's not easy being part of a vocation whose members are often depicted as disheveled, wild-eyed characters working single-handedly in dimly lit quarters on projects that are unlikely ever to come to fruition. Yet that is the stereotype that haunts many full- and part-time inventors. To transcend this stereotype and—what's more important—to obtain the recognition and support that they need to develop and market their best ideas, inventors can turn to a network of support organizations and services.

Most states have at least one inventors' organization, and some states have several. The groups, most of which have sprung up during the last decade, vary greatly in their form and organization. Some are loosely organized and staffed by volunteers; others are large assemblages run by full-time, salaried staffs. Many are registered within their states as nonprofit corporations.

Most of these organizations are less than 10 years old, and many have been formed within the last four years. Others, however, are older and more venerable. For example, the Philadelphia-based American Society of Inventors, which is among the nation's oldest inventors' societies, was established in 1951.

Membership in inventors' organizations ranges from 45 to 1500, and the groups' annual dues range from $25 to $45. Some of the organizations' rosters are made up solely of independent inventors. Other groups count patent attorneys, bankers, investors, and venture capitalists among their members. And despite the current emphasis on high-technology developments, inventors who are members of these groups are as likely to create household gadgets as they are to invent electronics-based equipment for industrial use.

One of the main goals of inventors' organizations is to provide a relaxed atmosphere in which inventors can meet with finance and marketing experts and learn to develop their ideas and realistically assess their commercial possibilities. "Inventing is a terribly lonely profession, so gathering information can be difficult to do," says Philip Knapp, president of the New York Society of Professional Inventors.

"It's an American myth that you have to be good at everything yourself," says Donald Margolis, a patent attorney and founder of the Rocky Mountain Inventors Congress. "You have to bring in other people with specialized knowledge to keep your project going." Margolis says that among his first bits of advice to clients is to join an inventors' support group.

Quarterly or monthly meetings are standard fare for inventors' groups; the meetings usually include a guest speaker from industry, government, or the university community. Many of the groups publish newsletters.

Some of the groups take on more ambitious programs. In addition to

The last decade has produced a network of support organizations and services whose goal is to dispel old stereotypes and offer inventors the assistance they need to keep creating.

The National Inventors Expo

Each February the Patent and Trademark Office sponsors the **National Inventors Expo**, which it holds in conjunction with National Inventors Day. At this year's show, 50 independent inventors and 20 corporations displayed their products. Because the exhibition is geared to the general public—more than 12,000 people attended this year—most of the inventions on exhibit are for consumers' use. All of the products displayed must be patented. For more information on the National Inventors Expo, contact Oscar Mastin, Office of Public Affairs, Patent and Trademark Office, Washington DC, 20231; phone (703) 557-3341.

Some inventors are hesitant to join inventors' organizations, in which they're encouraged to talk freely about their inventions, for fear of having their ideas stolen and marketed by others.

monthly meetings, for example, the Inventors Council of Hawaii holds four educational seminars each year. The Rocky Mountain Inventors Congress, which counts 170 engineers among its 260 members, cooperates with several other organizations to sponsor an annual conference. The 2-day meeting includes exhibits by inventors and local marketing and financing professionals. It also provides workshops that guide inventors through the travails of evaluating an invention's commercial potential; the workshops then cover how to license, finance, market, and promote the invention.

To promote its members' projects, the Palm Beach Society of American Inventors sponsors twice-yearly exhibitions. At one exhibition earlier this year, 49 members' ideas were on display. The exhibits are open to the public, and attendance averages 500. Citations are awarded to the best product in each of 13 categories, including categories for electrical, mechanical, chemical, and solar inventions.

Using a different method of publicizing its members' work, the Chicago-based Inventors Council mails its monthly publication to 1500 readers. The publication contains a classified advertising section in which members are allotted four free lines of copy to describe their work. The Inventors Council of Michigan also provides free advertising to its members—but in an unusual form. Its meetings feature a section called "standing classifieds," during which members with specialized skills or services can address the audience and offer their expertise to other members. Inventors who have run into trouble on some aspect of a project can also use this time to solicit assistance.

The recent interest in these inventors' organizations is due to more than just the groups' efforts to promote themselves and their members' work. The much-publicized entrepreneurial activity in the electronics industry has helped to raise the public's consciousness about inventors and has therefore increased interest in the organizations.

"One of the most significant changes is the perception that entrepreneurs are good," says George Lewett, chief of the National Bureau of Standards' Office of Energy-Related Inventions. "Everyone is aware of Silicon Valley and Route 128, and the general perception is that they resulted from technical creativity. As a result, the image of the inventor has improved." The positive publicity has also given inventors themselves an ego boost. "It's improved to the point where inventors now call themselves inventors. For years they preferred to call themselves engineers," according to Lewett.

Protecting against fraud

The services that inventors' organizations offer their members go far beyond monthly pep talks, however. For example, the organizations warn independent inventors against the ubiquitous invention-marketing company. For a fee that often runs to several thousands of dollars, such companies offer to evaluate, conduct a patent search for, and possibly even market an inventor's product. Many such companies are fraudulent and

A federal program for energy-minded inventors

Tailor-made for independent inventors, the Energy-Related Inventions Program (ERIP) evaluates ideas for saving energy, using energy more efficiently, or increasing energy from non-nuclear sources. The program is conducted by the National Bureau of Standards and is the result of legislation passed in 1974 to encourage research into and development of energy sources and alternatives.

An invention that is deemed to have commercial potential is referred by the Office of Energy-Related Inventions (OERI) to the Department of Energy. The OERI defines an invention as a concept, device, product, material, or industrial process. The review process takes five to nine months. In most instances, the inventor or small business is then eligible for a federal grant or contract award of $70,000 to $100,000.

Of the 23,000 inventions that have been submitted since the program's inception, the OERI has referred 360 to the Department of Energy for further evaluation. Over the last 10 years, the energy department has funneled more than $19 million to the recommended inventions. By 1983, 35 of the inventions had reached the marketplace, and sales revenues from the products totaled $178 million.

For more information on the program, contact the Office of Energy-Related Inventions, National Bureau of Standards, Gaithersburg, MD 20899; phone (301) 921-3694.

Inventors organizations

Support organizations for inventors are located in many US states, and the following list provides the addresses and available phone numbers for some of them. For more complete information, you can contact the Office of Energy-Related Inventions, National Bureau of Standards, Gaithersburg, MD 20899; phone (301) 921-3694.

California

Inventors of California
Norman Parrish
Box 158
Rheem Valley, CA 94570
(415) 376-7541

Colorado

Affiliated Inventors Foundation Inc
John Farady
501 Iowa Ave
Colorado Springs, CO 80909
(303) 635-1234

Rocky Mountain Inventors Congress
Box 3233
Boulder, CO 80307
no phone

Connecticut

Inventors Association of New England
Connecticut Chapter
Murray Schiffman
9 Sylvan Rd S
Westport, CT 06680
(203) 226-9155

Florida

Palm Beach Society of American Inventors Inc
Betty White
Box 26
Palm Beach, FL 33480
(305) 736-6594

Tampa Bay Inventors Council
MacNeill MacKay
805 W 118th Ave
Tampa, FL 33612
(813) 681-0010
(813) 933-9124

Georgia

Inventor Associates of Georgia
Hal Stribling
241 Freyer Dr NE
Marietta, GA 30060
(404) 427-8024
(404) 425-6907

Hawaii

Inventors Council of Hawaii
George Lee
Box 27844
Honolulu, HI 96827
(808) 595-4296

Illinois

Inventors Council
Donald Moyer
53 W Jackson, Suite 1041
Chicago, IL 60604
(312) 939-3329

Indiana

Inventors Association of Indiana
Randall Redelman
612 Ironwood Dr
Plainfield, IN 46168
(317) 745-5597

Massachusetts

Innovation Invention Network
Andrew Stidsen
13 Benjamin Rd
Worcester, MA 01602
(617) 799-4951

Inventors Association of New England
Donald Job
Box 335
Lexington, MA 02173
(617) 862-5008

Michigan

Inventors Council of Michigan
Downs Herold
University of Michigan
2200 Bonisteel Blvd
Ann Arbor, MI 48109
(313) 764-5260

Minnesota

Inventors Education Network
Marge Braddock
129 SE Bedford St
Minneapolis, MN 55414
(612) 379-7387

Inventors Technology Transfer Corp
Box 14-235
St Paul, MN 55114
(612) 379-7387

Minnesota Inventors Congress
Penny Becker
Box 71
Redwood Falls, MN 56283
(507) 637-2828

Society of Minnesota Inventors
Paul Paris
20231 Basalt St NW
Anoka, MN 55303
(612) 753-2766

Missouri

Inventors Association of St Louis
Roberta Toole
Box 16544
St Louis, MO 63105
(314) 534-7232

New Jersey

National Society of Inventors
Frank Sowa
Box 434
Cranford, NJ 07016
(201) 276-0213

New York

New York Society of Professional Inventors
State University of New York
Lupton Hall
Farmingdale, NY 11735
(516) 420-2397

Ohio

Inventors Council of Dayton
Leonard Smith
140 E Monument Ave
Dayton, OH 45402
(513) 435-1000
(513) 224-8513

Oklahoma

Oklahoma Inventors Congress
William Delay
6601 Broadway Extension, Suite 200
Oklahoma City, OK 73116
(405) 521-2401

Pennsylvania

American Society of Inventors
Henry Skillman
Box 58426
Philadelphia, PA 19102
(215) 546-6601

South Dakota

South Dakota Inventors Congress
Box 1113
Watertown, SD 57201
(605) 886-5814

Tennessee

Tennessee Inventors Association
Box 11225
Knoxville, TN 37939
no phone

Texas

Texas Inventors Association
Tom Workman
4000 Rock Creek Dr, #100
Dallas, TX 75204
(214) 528-8050

Utah

Intermountain Society of Professional Inventors
Box 1514
Salt Lake City, UT 84110
no phone

Washington

Inventors Association of Washington
Box 714
Bellevue, WA 98009
(206) 382-1925

Wisconsin

Midwest Inventors Group Inc
Steve Henry
Box 518
Chippewa Falls, WI 54729
(715) 723-5061

Workshops on the ins and outs of inventing

Each year the Office of Energy-Related Inventions (OERI) provides inventors with guidelines for developing and commercializing their products through a series of two-day seminars held throughout the country. The National Innovation Workshops are held in six cities each year and are jointly sponsored by the OERI, the National Society of Professional Engineers, the National Congress of Inventor Organizations, the American Intellectual Property Law Association, and the Licensing Executives Society. Registration is approximately $75. Six seminars are scheduled for 1987.

For more information, contact the Office of Energy-Related Inventions, National Bureau of Standards, Gaithersburg, MD 20899; phone (301) 921-3694 or the National Congress of Inventor Organizations, Box 158, Rheem Valley, CA 94570; phone (415) 376-7541.

Just as important as giving practical advice is the organizations' encouragement of members to enjoy the creative process.

have no intention of paying an invention any more than lip service. One inventors' group estimates that as many as 20% of its members have paid and lost money to such businesses. "Our minimum service is to warn people against them," says Donald Moyer, president of the Inventors Council.

Fraudulent front operations "move fast to stay ahead of the government," says Randall Redelman of the Inventors Association of Indiana. "They generally have one- or two-year lifespans. The government no sooner puts one of these companies out of business than two more spring up." Redelman, an engineering consultant, has first-hand knowledge of the threat such companies pose to unknowing inventors. When he was 18, he paid $1000 to a firm that agreed to market a kitchen device he had developed. One year later, after hearing little from the company other than that it had reviewed his product and found it to have commercial potential, Redelman reviewed the contract he had signed and found that simply by notifying him that it deemed his invention marketable, the company had fulfilled the terms of the contract.

Similar experiences, as well as the fear of having their ideas stolen and marketed by others, make some inventors wary of anyone who shows interest in their ideas and of any environment—such as inventors' group meetings—in which they're encouraged to talk freely about them. Three years ago, when Mark Ratner became editor of *New Products Marketplace,* a newsletter that publicizes technological developments in university, government, and industry research labs, one of his goals was to make the publication a vehicle for promoting the work of independent inventors. But after talking to numerous inventors' groups, Ratner says, "we've gotten next to nothing." Many inventors are "paranoid" about talking about their inventions, he says, because of their past experiences. Ratner sympathizes, however, with inventors who have been duped by such companies, and he shares their distrust of such businesses. "When I've called to ask [invention-marketing companies] about their track records, I've never gotten satisfactory results."

Inventors' organizations say they aim to help heal the wounds caused by fraudulent invention-marketing businesses and to draw inventors out into a supportive environment. Just as important as giving practical advice, however, is the organizations' encouragement of members to enjoy the creative process—even if no profit is involved. "Typically, every inventors' invention is his baby; nothing is more important or more beautiful to him than his invention," says Margolis. The most important contribution inventors' groups can make to inventors is to keep the creative flame burning. **EDN**

Article Interest Quotient
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1986 Editorial Calendar and Planning Guide

Issue Date	Recruitment Deadline	EDN Editorial Emphasis	EDN CareerNews
Nov. 13	Oct. 23	Wescon '86 Show Issue; Op Amps; CAE; Semicustom ICs (CAE- related*); Artificial Intelligence (CAE-related*)	Closing: 11/3 Mailing: 11/25
Nov. 27	Nov. 6	Microprocessor Technology Report & Directory; CAE; Passive Components	
Dec. 11	Nov. 18	Product Showcase—Volume I; ICs & Semiconductors; Hardware & Interconnection Devices; Power Supplies/Sources; Software; Literature on Computers & Peripherals, Components, Test & Measurement Instruments, International Products	
Dec. 25	Dec. 4	Product Showcase—Volume II; Computers & Peripherals; Components; Test & Measurement Instruments; International Products; Literature on ICs & Semiconductors, Hardware & Interconnection Devices, Power Supplies/Sources, Software	

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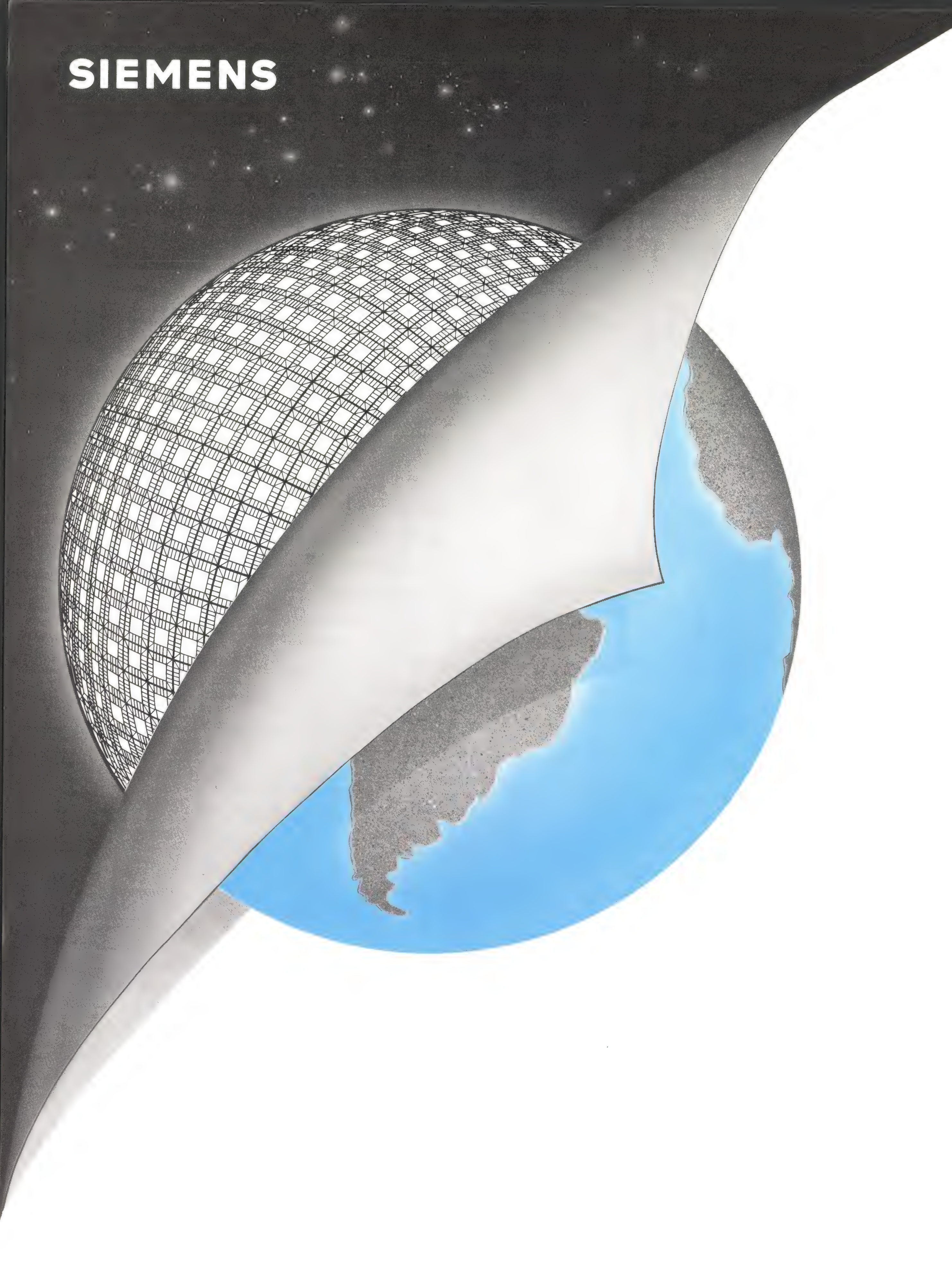

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- ☐ Systems engineering of imaging infrared detection systems and guidance and control concepts
- ☐ Digital electronics and/or control systems

Test Engineers

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Reliability Engineers

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The above Test and Reliability opportunities require a Bachelors degree in Electrical or Mechanical Engineering or Physics, with a minimum of 3 years of related experience in complex defense-oriented manufacturing environment.

Specifications Engineer

Responsible for preparing specifications and changes to support technical data packages for components and assemblies. Requires BSEE and experience in preparing and controlling specifications and a working knowledge of MIL-STD-490.

Product Engineers

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Senior LSI Engineers — Ideal candidates will be IC Designers with 2-4 years experience in the design of processing and control parts for graphic and imaging products.

Senior Engineers — Will develop/maintain graphics and imaging software for IBM PC/XT and AT products. Minimal requirements include BSCS plus 2 years related experience in the areas of I/O drivers for advanced peripheral device controllers (i.e. raster image processors, display controllers and image scanners).

Product Specialist — Responsible for technical program coordination, applications engineering, customer and field technical support. Also involves technical training of field personnel during product launch and coordination of documentation/software release to the field. Requires BSEE/CS with application software background in PC-based graphics and/or desktop publishing.

Senior IBM Program Manager — Will administer multiple IBM programs, from conception through long-term production. Requires a Bachelors degree in Engineering Technology, a minimum of 3-5 years computer industry program management experience plus strong interpersonal, communication and supervisory skills. MBA desired.

Senior Firmware Engineer

Will develop firmware and diagnostics for PC disk controllers. Minimal requirements include BSEE/CS plus 5 years related experience in peripheral controller firmware design and diagnostics. Experience with IBM PC BIOS, Intel 8049, 8051, 8086 microprocessors, 'C' and 8086 assembly languages preferred.

Senior Hardware Engineer

Responsibilities include hardware design/sustaining for floppy/hard disk controllers. Knowledge of IBM PC products, BSEE/CS, and a minimum of 5 years experience are essential. Familiarity with firmware desired.

Senior LSI Product Engineer

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Process Engineers — Will be responsible for diffusion ion implantation, photolithography and thin films. Requires BS degree and 2-5 years experience, including NMOS/CMOS.

Device Engineers — Qualified individuals will have a technical degree plus 2-5 years experience in NMOS and CMOS device electrical failure analysis.

Principal Software Engineer

Will develop communications software for microprocessor environments. Requires 5-7 years experience, a technical degree and knowledge of X.25 or 150 protocols.

Principal Hardware Engineer

Will develop LSI analog circuits for communications environments. Requires a technical degree and knowledge of phase loops.

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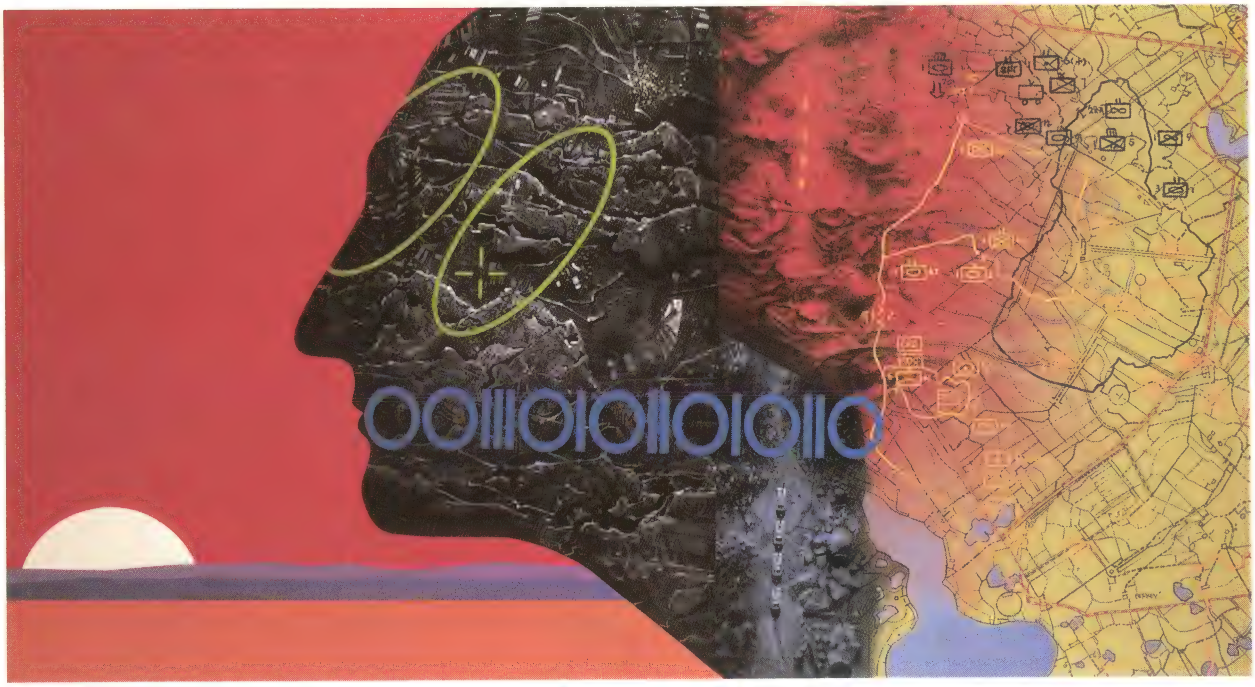

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Radar Systems

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LOOKING AHEAD

EDITED BY GEORGE STUBBS

Semiconductor growth rate to be 15% to 1995

Though annual growth rates in the semiconductor industry will not match the giddy levels of previous years, average rates to 1995 are expected to be a healthy 15%, according to the market-research firm Henderson Ventures (Los Altos, CA). During the period 1985 to 1995, consumption of semiconductor devices by concerns in so-called free-world nations will increase from $29 billion to $117.5 billion.

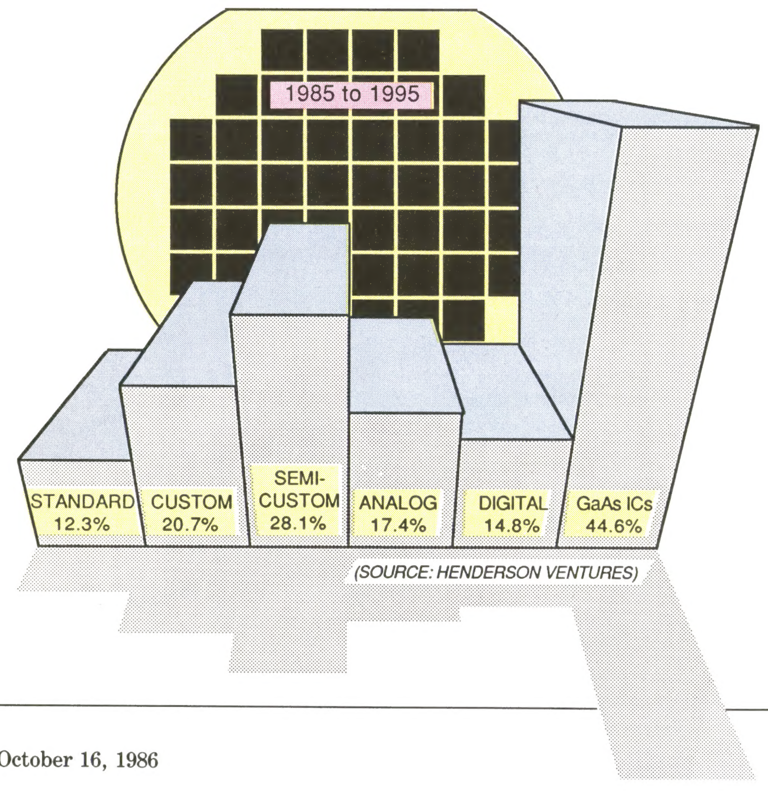
Ken Taylor, the research firm's director of semiconductor research and consulting, reports that companies devoted to production of silicon-based, standard digital ICs can expect single-digit growth, as gallium arsenide finally makes its long-awaited gains, and as standard products give way to custom, semicustom, and application-specific ICs.

Taylor also believes ICs must "live closer to the real world" in the future; as a result, the growth of analog ICs will outpace that of their digital counterparts over the next 10 years. Spurring this growth will be pattern-recognition applications involving speech, touch, and vision signal analysis.

During the 10-year period specified by the forecast, the US will maintain its lead in the consumption of semiconductor devices, though the share will slip from 42 to 40%, according to Henderson Ventures. Western European nations will lose some of their share of semiconductor consumption while Far Eastern nations and countries in the rest of the noncommunist world will increase their use.

Henderson Ventures predicts that semiconductor suppliers will need higher levels of R&D and capital equipment expenditures in order to remain competitive, leading to more vertical integration. Use of advanced VLSI devices will grow, and OEMs will form strategic alliances and acquire in-house semiconductor manufacturing facilities. As a result, captive production of semiconductors will increase from 19.3% in 1985 to 24.2% in 1995.

ANNUAL GROWTH RATES FOR SEMICONDUCTOR MARKET SEGMENTS



(SOURCE: HENDERSON VENTURES)

VLSI design centers aid system designers

Growing demand for VLSI design expertise will lead makers of large computers and computer-based systems to regional VLSI design centers. By 1990, reports Electronic Trend Publications (ETP), a Saratoga, CA-based research company, these regional design centers will be giving assistance to more than 60% of all system designers in projects involving application-specific ICs (ASICs), and the centers will have a hand in 75% of the expected $7.2 billion in ASIC sales.

According to ETP, there are 3000 to 4000 expert IC designers in the world, and 65% of them are employed by semiconductor manufacturers. This population has remained relatively stable for the last 10 years while the number of system designers has tripled in that time and will double again by 1990, says ETP. This changing ratio of system designers to IC designers has increased the demand for IC design expertise, and the emergence of the regional VLSI design center is a direct result.

Regional VLSI design centers provide a range of services, including engineering support, training, and initial consultation. In the interest of time, a customer may simply turn a design project over to the center, where its IC designers can quickly come up with the IC and transmit the fabrication and testing data to a manufacturer. Customers may also use the centers to gain familiarity with IC fabrication and design processes and with the use of computer-aided engineering equipment.

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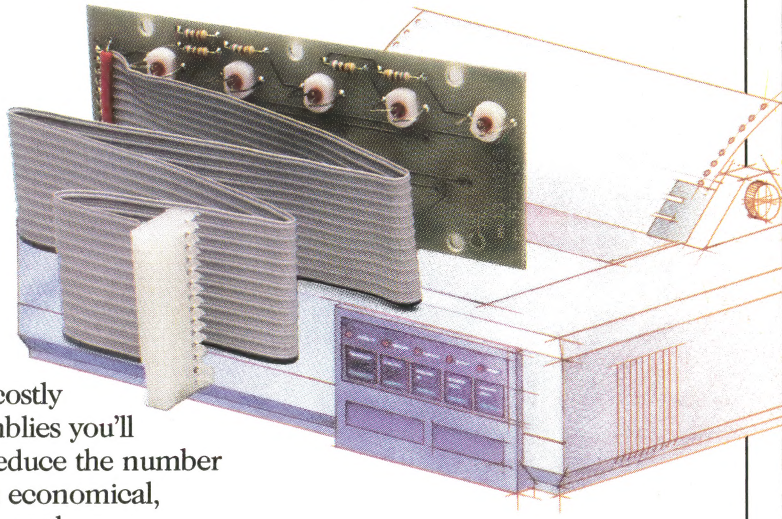

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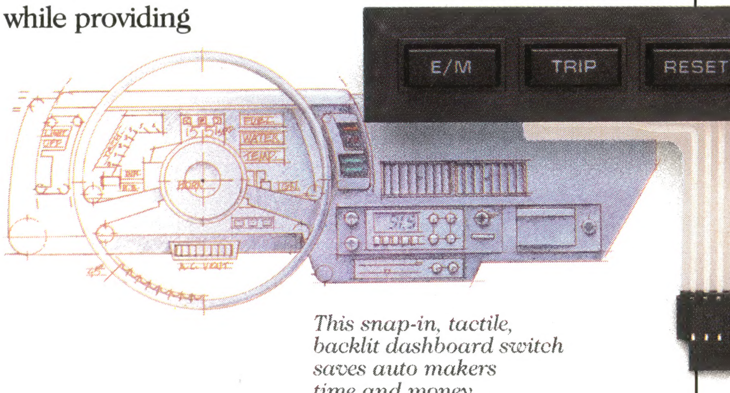

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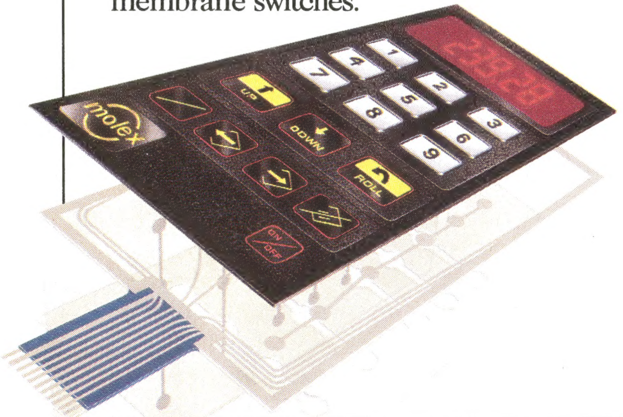

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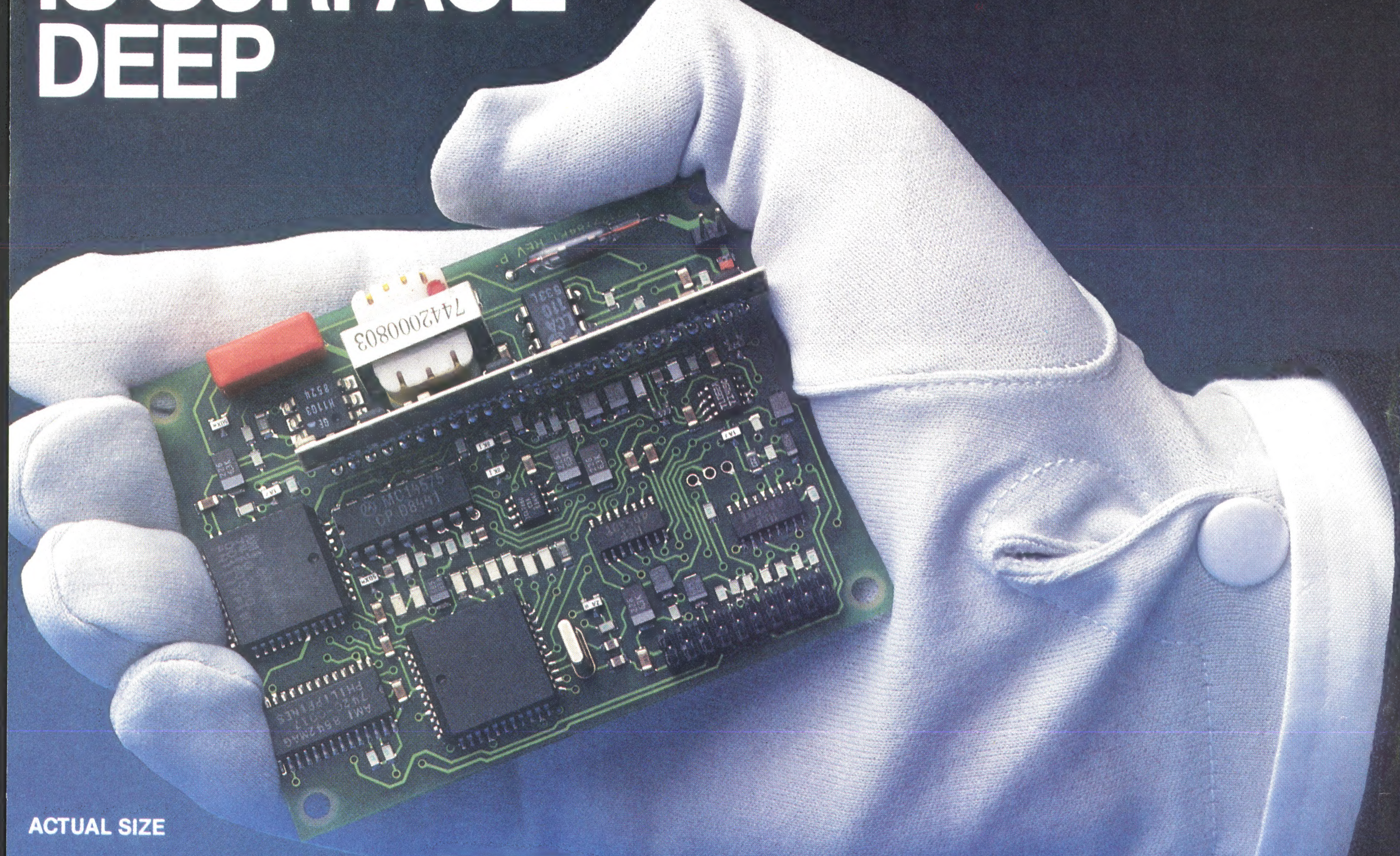

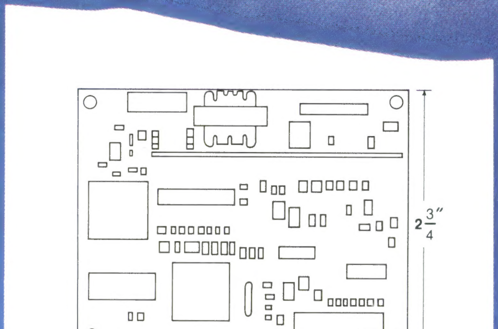

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